Flexible Power control in Large Power Current Source Conversion

Nick Murray

A thesis presented for the degree of
Doctor of Philosophy
in
Electrical and Computer Engineering
at the
University of Canterbury,
Christchurch, New Zealand.

2008

ABSTRACT

This thesis describes a new concept, applicable to high-power current-sourced conversion (CSC), where a controllable firing-angle shift is introduced between series and parallel converters to enable independent active and reactive power control. The firing-shift concept solves a difficult problem, by giving thyristor based CSCs the control flexibility of pulse-width modulated (PWM) converters, but without a loss in efficiency or rating. Several configurations are developed, based on the firing-shift concept, and provide flexible, efficient solutions for both very high power HVDC transmission, and very high current industrial processes.

HVDC transmission configurations are first developed for 4-quadrant high-pulse operation, based on the series connected multi-level current reinjection (MLCR) topology. Independent reactive power control between two ends of an HVDC link are proven under firing-shift control, with high-pulse operation, and without on-load tap changing (OLTC) transformers. This is followed by application of firing-shift control to a bi-directional back-to-back HVDC link connecting two weak systems to highlight the added dc voltage control flexibility of the concept.

The fault recovery capability of an MLCR based ultra-HVDC (UHVDC) long distance transmission scheme is also proven under firing-shift control. The scheme responds favourably to both ac disturbances and hard dc faults, without the risk of commutation failures and instability experienced during fault recovery of line-commutated conversion.

The two-quadrant capability of very high current rectification is also proven with configurations based on phase-shifted 12-pulse and MLCR parallel CSCs. The elimination of the electro-mechanical OLTC/satruable reactor voltage control, the high-current CSC's biggest shortcoming, greatly improves controllability and with firing-shift control, ensures high power-factor for all load conditions. This reduces the reactive power demands on the transmission system, which results in more efficient power delivery.

ACKNOWLEDGEMENTS

Firstly, my heartfelt thanks must go to my supervisors, Associate Professor Neville Watson, Emeritus Professor Jos Arrillaga, and Dr. Yonghe Liu, three very wise men indeed. Throughout my thesis you've given me encouragement, friendship, advice and inspiration, and with your help, I've learnt more than I ever thought possible in a three year period. Your office doors were always open, whether for philosophical discussions or just a chat, you always had time for me, and for that I am truly grateful.

Also, thanks must go to Reuben Cohen, my high school Calculus teacher and friend, whose philosophical discussions on Pythagoras, hypercubes and the age of the universe helped inspire my tertiary studies.

I am indebted to my many postgraduate colleagues, coworkers and friends. To Chris Penniall and the Penniall family, Lance Frater, Simon Bell, Ben Parry, the Rossallen family, Ken Smart, Dave Healy, Pieter Kikstra, Jac Woudberg, and the late Ron Battersby, you've all contributed so much during my time here at the University of Canterbury.

I'd also like to express my gratitude to Joseph Lawrence and the Electrical Power Engineering Centre (EPECentre) for their financial support; without the EPECentre Postgraduate Scholarship, none of this would have been possible.

Finally I'd like to thank my family, Mum, Dad, Rob, Niki, and my beautiful wife Stacey, for their love, patience, understanding and support. To them I dedicate this thesis.

CONTENTS

LIST OF FIGURES

LIST OF TABLES

GLOSSARY

Abbreviations

ac	Alternating Current
BTB	Back To Back
CCC	Capacitor Compensated Conversion
CSC	Current Source Converter
dc	Direct Current
FACTS	Flexible AC Transmission System
EMTDC	Electromagnetic Transients including DC
FFT	Fast Fourier Transform
GTO	Gate Turn Off Thyristor
HVAC	High Voltage Alternating Current
HVDC	High Voltage Direct Current
IGBT	Insulated Gate Bipolar Transistor
IGCT	Integrated Gate Commutated Thyristor
LCC	Line Commutated Conversion
MLCR	Multi Level Current Reinjection
MLCR-CSC	Multi Level Current Reinjection Current Source Converter
NPC	Neutral Point Clamped
OLTC	On Load Tap Change
pu	per unit
PI	Proportional and Integral
PID	Proportional, Integral, and Derivative
PLL	Phase locked loop
PSCAD	Power systems computer aided design
PWM	Pulse Width Modulation
RCD	Resistor Capacitor Diode
RMS	Root Mean Square
SCR	Short Circuit Ratio or Silicon controlled rectifier
SMES	Superconducting Magnetic Energy Storage

STATCOM	Static Synchronous Compensator
SVC	Synchronous Var Compensator
THD	Total Harmonic Distortion
UHVDC	Ultra High Voltage Direct Current
VSC	Voltage Source Converter
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

Symbols

α	firing angle of the main bridge rectifier switches
α_{1A}, α_{1B}	Sending end converter group firing angles
α_2	Receiving end converter firing angle
$\Delta\alpha_{s_{1p}}$	Incremental sending end firing angle for converter 1 active power channel
$\Delta\alpha_{s_{1q}}$	Incremental sending end firing angle for converter 1 reactive power channel
$\Delta\alpha_{s_{2p}}$	Incremental sending end firing angle for converter 2 active power channel
$\Delta\alpha_{s_{2q}}$	Incremental sending end firing angle for converter 2 reactive power channel
ω	Angular frequency of the source
θ	Phase displacement between the converter system output current and voltage
A_r	Receiving end converter transfer function
A_s	Sending end converter transfer function
i_{Yd}	DC side current of the Y connected bridge
I_1	Sending end current
I_2	Receiving end current
I_{1A}, I_{1B}	Sending end converter group currents
I_{2A}, I_{2B}	Receiving end converter group currents
$I_{a\Delta}$	Output line current of the Δ connected bridge
I_{aY}	Output line current of the Y connected bridge
I_{aYn}	n^{th} harmonic component of the line current of the Y connected bridge
I_{A1}	Fundamental component of the converter system output current
I_{An}	n^{th} harmonic component of the converter system output current
$I_{B\Delta}$	DC side output current of the Δ connected bridge
I_{BY}	DC side output current of the Y connected bridge
$I_{ca\Delta}$	Phase current of the Δ connected bridge
$I_{ca\Delta n}$	n^{th} harmonic component of the phase current of the Δ connected bridge
I_d	DC side current
$I_{d_{6p}}$	DC current in a 6-pulse rectifier
I_{s1}, I_{s2}	Sending end group currents

L_d	Inductance of the dc side
P	Active power
P_1	Sending end source Power
P_d	DC Power
P_{ref}	Active power reference order
P_{sp}	Specified Power
P_{T_r}	Receiving end active power at the converter terminal
P_{T_s}	Sending end active power at the converter terminal
Q	Reactive power
Q_1	Sending end reactive power
Q_2	Receiving end reactive power
Q_{ref}	Reactive power reference order
R_d	Resistance of the dc side
R_1, R_2	Receiving end converter units
S	Converter system nominal apparent power
S_1, S_2	Sending end converter units
THD_I	Total harmonic distortion of the converter system output current
V_1,V_s	Sending end source voltage
V_2 ,V_r	Receiving end source voltage
V_o	dc load back emf
V_{T_a}, V_{T_b}, V_{T_c}	Terminal voltage of phase ‘a’,‘b’, and ‘c’ respectively
V_{T_s}	Sending end converter terminal voltage
V_{T_r}	Receiving end converter terminal voltage
V_d	DC voltage
V_{d_r}	Receiving end dc voltage
V_{d_s}	Sending end dc voltage
X_1, X_s	Sending end series ac system reactance
X_2, X_r	Receiving end series ac system reactance

Chapter 1

INTRODUCTION

Humankind's voracious appetite for energy is increasing faster than ever before, with world electricity usage tripling over the last 30 years [1], the greatest increases in China and India. Satisfying this demand requires large scale new generation, and an increasing reliance on efficient transmission of vast quantities of energy from remote generation resources to the largest load centres. At powers over 1000MW with distances of over 700 km HVDC transmission is generally preferred to HVAC [2] where the advantages of lower overall losses and smaller transmission corridor outweigh the complications of rectification and inversion.

The general trend in long distance bulk power transmission is toward greater power transfer at higher voltage, for increased efficiency and to better match transmission capability to the ratings of remote generation schemes. The powers and distances under consideration are up to 6000 MW and 2000 km respectively and the voltage selected by the planners for these projects is ±800 kV Ultra high voltage DC (UHVDC). With higher power, there is a need for improved controllability, to better control power transfer, to increase efficiency, and to quickly respond to changing network conditions.

At present large HVDC power interconnections are still line commutated converter (LCC) based. Although this technology provides greatest conversion efficiency, it suffers from limited control flexibility, and has remained largely unchanged for almost 50 years. With heavy reactive power demands and low order characteristic harmonics, LCC in its present form is far from ideal for future large-power flexible converters.

The term "large" requires a reference for its interpretation. In this respect three rating components are involved, namely voltage, current and power. Understandably, large power ratings can only be achieved by a corresponding large current and/or voltage rating, but not necessarily both. While large power transmission uses high voltage and relatively low current in order to reduce power losses, some industry processes (such as aluminium smelting), require very high current and comparatively low voltage.

At very high currents (in excess of 100 kA) and with ratings of up to 500 MW, the industrial

processes predominantly use diode rectifiers and on-load tap-changing (OLTC) transformers coupled with saturable reactors for dc side control. This electro-mechanical combination control limits control capability and has reactive power and harmonic problems similar to those of HVDC conversion.

New topologies to improve on converter flexibility have been proposed but with more controllability comes added circuit complexity, which ultimately results in reduced efficiency. The type of switch used largely determines the controllability and efficiency of the converter. The desired characteristics for a converter switch are thus, low on-state voltage drop, low switching losses, fast switching time, high power rating, high breakover voltage, simple gate driving and for flexibility, turn-off capability. Given the high voltage or current of modern converters, the ease of driving many series connected switches (or parallel in the case of high current) and any auxiliary voltage balancing components (and their associated losses) must also be considered.

Present commercially available switch ratings for line-commutated switches are 6.5 kV/3.4 kA (ABB), 8.0 kV/2.6 kA (Eupec) and 12 kV/1.5 kA (Mitsubishi), which although lacking control flexibility feature the lowest on-state losses. Self-commutated switches are offered by several manufacturers, with ratings of 3.3 kV/1.5 kA (Eupec), 5.2 kV/2 kA (Fuji) for insulated gate bipolar transistors (IGBTs) and 6.5 kV/1.3 kA (ABB), 6 kV/6 kA (Mitsubishi) for integrated gate commutated thyristor (IGCT). Even though improvements in self-commutated switch ratings may eventually match those of their line-commutated counterparts, their on-state volt-drop will remain higher (particularly for the IGBT) due to their more complex switch structure. Therefore, in each case a compromise must be made between efficiency and control flexibility.

In recent years, multi-level and multi-pulse converter topologies have been suggested as flexible and efficient converter solutions. Much emphasis has been placed on voltage source conversion (VSC) particularly in FACTS devices [3], with multi-level capacitor clamped [4, 5], neutral point clamped (NPC) [6, 7], and cascaded H-bridge [8, 9] configuration proposals. The topologies offer control flexibility and the multi-level switching concept reduces the switch voltage stresses and balancing problems of earlier VSCs. Still, the multiple levels add to the number of components required, with each increase in level squaring the number of capacitors required for capacitor clamped VSC, and clamping diodes for the NPC VSC. The cascaded H-bridge configuration has gained popularity in STATCOM applications, but is unsuitable for HVDC because of the need for many isolated dc sources. A recent two-part publication [10, 11] removes the dependence on isolated sources and successfully applies the improved H-Bridge VSC to HVDC transmission.

All VSCs suffer one major limitation, in that they lack direct controllability of dc voltage. Moreover, with overhead lines offering the only economic solution for long distance (land based) transmission, a dc fault on a VSC converter cannot be directly contained (owing to the dc capacitor and free-wheeling diodes) and the converter must be isolated by ac circuit-breaker action to prevent converter damage. The long recovery time for such a fault is primarily why

VSC HVDC is cable based. If VSC dc voltage control is required, as is the case in high current industrial applications, a dc chopper and inductor must be added, a solution that is inefficient and uneconomical at high voltages.

Current source converters (CSCs) on the other hand have large dc smoothing reactors that limit the current peak, and have direct dc current control to quickly contain a dc fault. CSCs have remained the domain of line-commutated conversion, with the inductor seen as more expensive and larger than equivalent rated VSC capacitors [12] and the need for bidirectional blocking switches (requiring IGBTs with series connected diodes at additional loss).

LCC CSCs do suffer from large reactive power absorption, owing to the thyristor firing and commutation angles, which can cause stability problems in weak systems. Installing capacitors in series with the converter (a solution called capacitor commutated conversion or CCC) [13] greatly reduces the reactive power demands, providing favourable characteristics at full rated power transfer. The CCC has been used successfully to interconnect Argentina and Brazil with two back to back (BTB) 1100 MW HVDC ties. The BTB CCC links the 50 Hz and 60 Hz ac systems with low short-circuit capacity without the stability issues of conventional LCC [14]. Despite the advantages, the topology is still based on LCC switching, with the same limited control freedom.

The method of switching (or gating) has a pronounced effect on overall converter efficiency. LCCs by way of their synchronous switching restriction, have the lowest switching losses of all converters, but generate low order harmonics characterised by the switching frequency. The characteristic harmonic order may be increased by suitable transformer phase-shifts, which are applicable where power ratings require several series or parallel connected converters. However, HVDC converters are restricted to a 30° shift (star primary star/delta connected secondaries) because the transformer connections required for further shifts are impractical at high ac voltage. Thus LCC conversion needs large ac filters to attenuate the low order harmonics produced.

Increasing the switching frequency well above fundamental, together with pulse-width modulation (PWM) provides control of fundamental voltage from a fixed dc source in self-commutated VSC conversion, and permits selective cancellation of low order harmonics. PWM characteristic harmonics are shifted to multiples of the switching frequency, which are usually in the kHz range. The dc voltage ripple frequency is also increased, and this allows the size of the dc capacitor to be reduced.

While PWM provides a higher level of control flexibility and a reduction in the harmonic filtering requirements, some filters need to be provided to minimise radio frequency interference (RFI). The high PWM switching frequency, and resulting rapid switching of the ac bus voltage (high $\frac{dV}{dT}$) puts strain on switches and wound components which are susceptible to damage by repetitive transient stresses. PWM schemes also suffer from high switching losses which in some cases may

outweigh the switch on-state losses [15]. Accordingly, the ratings of present PWM schemes are restricted to 3-level and 350 MW in HVDC transmission, thus making them unsuitable for either very large HVDC or very high current applications.

A ripple reinjection concept, first proposed in [16] and applicable to CSCs showed promising harmonic performance with a small increase in switching complexity, but a corresponding reduction in filtering requirements. By appropriately distributing current between two parallel connected LCC rectifiers via a multi-tapped reactor, the effective pulse number could be multiplied. The parallel connection is well suited to higher current applications, but is of limited use in long distance HVDC transmission. A later publication [17] proposed a series connected current reinjection scheme, where ac current was either added to or subtracted from the dc current to increase the pulse number. An appropriately wound single phase transformer with dc blocking capacitors and groups of back to back connected switches provided the reinjection path for pulse increase. More recently, improvements in switching technology and ratings have enhanced the reinjection concept by proposing multi-level current-reinjection (MLCR) in both series and parallel configurations [18], with self-commutated switches included in the reinjection path. Although the switches have higher losses, they are of lower voltage and current rating, and conventional thyristors are still used in the main bridges. The thyristors are freed of a commutation angle constraint by the self-commutated switches which also give an added degree of control freedom by allowing an MLCR equipped CSC to work in all 4 operating quadrants.

While the MLCR CSC summarised above is capable of 4-quadrant operation, and can thus generate reactive power in quadrants 1 and 2, the active and reactive powers are still intimately linked by the use of a single converter firing-angle. Generation of reactive power can be advantageous in supporting ac system voltage, but can damage insulation and equipment if the system voltage is not maintained within limits. This limits the MLCR CSC suitability as a stand alone flexible converter topology. The VSC in contrast, although excluded because of its lower ratings, efficiency and lack of dc voltage control, offers true 4-quadrant control. VSC converter active power is controlled by manipulating ac voltage angle, whilst reactive power is controlled independently (within its operating limits) by regulating ac voltage magnitude.

Eduardo Weichmann et. al. proposed the grouping of converters for high current applications using PWM switching [19]. The same authors discussed the advantages of staggering converter phase-shifts to achieve high power-factor high current operation [20], while a further publication [21] reviewed high current topologies with different switch structures and concluded that those using thyristor switches offered the best overall solution.

Of the thyristor switched converters discussed in the literature, no configurations have yet been proposed that give full 4 quadrant control flexibility to rival their PWM equivalents. The objective of this thesis is to enable true 4 quadrant thyristor based conversion, whilst retaining the high efficiency and power rating of conventional LCC topologies.

True 4 quadrant operation, where active and reactive power are fully and independently controllable within the converter rating, represents complete converter flexibility. In the case of HVDC transmission it will give a converter the freedom to operate with maximum dc link voltage at all power transfer levels, thus minimising dc losses under all operating conditions. This freedom, in both HVDC and high current applications, means a converter's reactive power (and therefore power-factor) may be controlled to permit ac power transfer into or out of the connected ac systems at maximum efficiency. This constitutes a minimum ac current for a specified active power transfer, which in HVDC transmission is unity power-factor at the generator's terminal. In weak networks (those with low short-circuit capacity) a slightly reduced converter efficiency may be tolerated in order to generate surplus reactive power and improve voltage stability, reliability or power quality of the system as a whole.

As stated previously, no single converter topology discussed above solves the flexibility-efficiency paradigm with respect to high power conversion. The logical base topology for further development is the CSC and is the only practical option in both extremely high dc current applications and HVDC overhead transmission. The MLCR and CCC CSC configurations both have clear advantages over conventional LCC, with the 4-quadrant capability of the MLCR converter being preferable to the CCC, which remains essentially a two quadrant configuration. With large power conversion, multiple converters are required, in either series or parallel, to achieve the voltage and current ratings respectively. This gives provision for further control flexibility by suitable MLCR connection.

This thesis examines the characteristics of current source conversion and proposes several new high-pulse, high power-factor HVDC schemes and industrial applications that exhibit the controllability of self commutated PWM rectification and inversion, but with the ratings and efficiency of traditional line commutated converters.

1.1 THESIS OUTLINE

This thesis is separated into two sections, the first and the subject of chapters 2 to 4 examines rectification and inversion in HVDC configurations, while the second section deals with extremely high current applications in electrowinning (smelting) and chemical production and is the focus of chapters 5 to 7. Each chapter is further summarised below.

Chapter 2 discusses the series connected multi-level current-reinjection (MLCR) scheme in 48-pulse equivalent configuration and its applicability to HVDC transmission. With a controllable firing-shift maintained between the series connected MLCR converters at both ends of the link, independent reactive power control is realised.

Chapter 3 extends the series connected MLCR based firing shift control method developed in

chapter 2 to include full independent dc voltage control as well as reactive power control, and applies the theory to a back to back (BTB) link interconnecting two weak power systems.

Chapter 4 summarises the development of a high power-factor Ultra high voltage dc (UHVDC) long distance transmission system and its performance under both single phase and three phase faults. The system's performance under hard dc faults is also given, including detection, fault clearing and recovery.

Chapter 5 introduces the aluminium smelter and the multi-parallel thyristor-based high power-factor configuration and its applicability to extremely high dc current loads. The analysis is made with reference to an aluminium smelter.

Chapter 6 covers extremely high current ac to dc conversion based on the parallel MLCR in a high power-factor configuration. Several methods are proposed to further improve the reactive power flexibility without increased rating. The control methods are proven on a simulated smelter.

Chapter 7 presents the hybrid parallel phase-shifted Thyristor MLCR high current rectifier.

Chapter 8 provides general conclusions and future work in the area of high power-factor current sourced conversion.

Chapter 2

FLEXIBLE REACTIVE POWER CONTROL IN MULTI-GROUP CURRENT-SOURCED HVDC TRANSMISSION

2.1 INTRODUCTION

Owing to the structural simplicity and four quadrant power controllability, PWM (Pulse Width Modulation) conversion has so far been the preferred option for self-commutating medium power HVDC Transmission [22, 23]. However, this technology is less suited to large power ratings and long distances, due to higher switching losses and to the rating limitations of its main components (namely the power transistor switch and underground cable). Thus the interchange of large quantities of power between separate power systems and the transmission of power from remote generating stations are still based on the principle of line-commutated current source conversion.

Multi-level VSC configurations have been presented as possible alternatives [24, 25] to PWM-VSC Transmission, but their structural complexity has been the main obstacle to their commercial implementation. A recent proposal, the multi-level current reinjection (MLCR) concept [26], simplifies the converter structure and permits the continued use of conventional thyristors for the main converter bridges [27].

The main advantage of self over natural-commutation in HVDC Transmission is the ability to control independently the reactive power at each end of the link, a property that can not be achieved by MLCR-based (or any other multi-level) configuration when using only one double-bridge converter group. However, interconnections of large power ratings will normally use two or more twelve-pulse converter groups and these can be controlled independently from each other without affecting the output voltage waveform. This fact constitutes the basis of the new control scheme proposed here. When the operating condition at one end of the link alters the reactive power balance at this end, the firings of the two groups at the other end are shifted with respect to each other in opposite directions to keep the power factor constant. The new control concept gives the MLCR configuration (summarised in Appendix B) the flexibility until now only available to PWM-VSC Transmission.

2.2 INTERDEPENDENCE OF REACTIVE POWER UNDER CONVENTIONAL CONTROL

PWM provides fully independent controllability of the converter voltages (and therefore reactive power transfers) on both sides of the link.

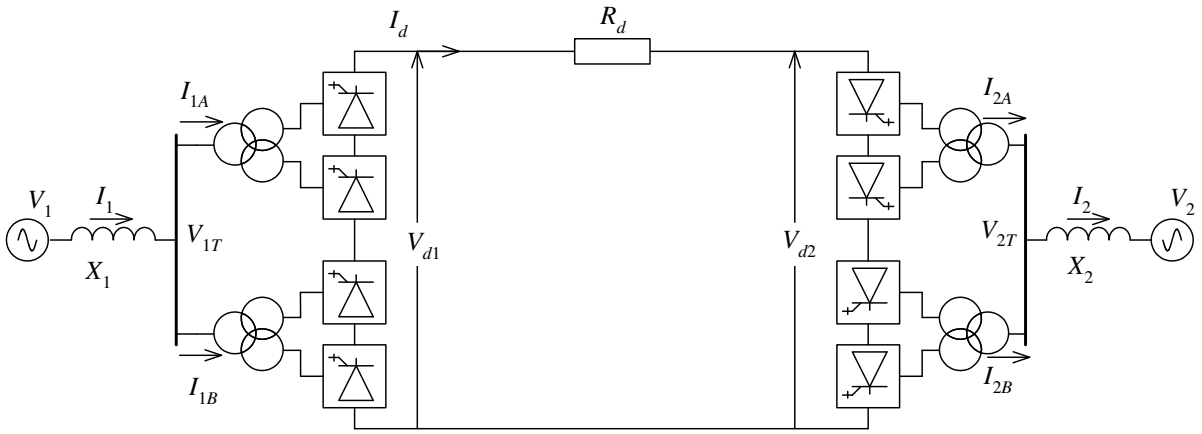


Figure 2.1 Simplified diagram of a DC link connecting two AC systems

This capability is not available to multi-level configurations under the present control strategies. For instance, if extra reactive power is needed at the receiving end to maintain the ac terminal voltage constant, the firing-angle (α) is increased and, therefore, the dc voltage reduced. To continue transmitting the specified power under this condition, the sending end station must also reduce its dc voltage. The dc voltage reduction is implemented by a corresponding increase in the firing-angle of the two converter groups; this action will force an unwanted extra injection of reactive power and, thus, an increase of ac terminal voltage at this end. Such condition would not occur if some PWM control were to be added to the multi-level configurations. However the use of PWM is currently limited to three-levels and is only used in voltage source conversion schemes.

2.3 THE MULTI-GROUP FIRING-SHIFT CONCEPT

The exchange of reactive power between the converter and ac system is determined by the sine of the firing-angle (α). Altering α has an immediate effect on the dc voltage level and, thus, to maintain the specified dc power transfer through the link, a corresponding change of firing-angle must be made at the other end, which in turn affects its reactive power exchange with the ac system. Therefore, under conventional converter control, the reactive powers injected at the two ends of a multi-level CSC link are interdependent.

In multi-level CSC HVDC interconnections with two twelve pulse groups per terminal (such

as shown in Figure 2.1) the same current waveform is produced by each of the 12-pulse converter groups, and thus the total output current waveform remains the same if a phase-shift is introduced between the firings of the two groups constituting the converter station.

When a change of operating conditions at the receiving end demands more reactive power from the converter, and thus reduces the dc voltage, shifting the firings of the two sending end converter groups in opposite directions provides the required dc voltage reduction, while maintaining the reactive power constant (due to the opposite polarity of the two firing-angle corrections). A relatively small change of active power will be caused by the variation of the fundamental current produced by the shift, but this change can be compensated for by a small extra correction of the two firing-angles.

For a converter to operate in the firing-shift mode (which in the above example is the sending end converter), the firing instants of one group (say group A) is kept on the positive side (thus providing reactive power), while the second group (say group B) may act as a source or sink of reactive power (i.e. the firing-angle may be positive or negative).

2.3.1 Steady State operation

To simplify the explanation of the steady state characteristics only, the sending end operates under firing-shift control, while the receiving end uses a common firing-angle for the two converter groups. The generalised method with firing-shift at both ends will be used in the dynamic simulation.

Also, as shown in Figure 2.1, the interconnected ac systems are represented as simplified Thevenin equivalents, i.e. V_1, X_1 andV_2, X_2.

At the receiving end the control specifications are the terminal ac voltage (V_1) and the dc voltage (V_d), while those at the sending end are the dc power transfer (P_{d1}^{sp}) and the reactive power (Q_1).

Receiving end:

As at this end no firing-shift control is exercised, the firing-angle will be the same for the two converter groups (i.e. $\alpha_{2A} = \alpha_{2B} = \alpha_2$).

The dotted lines in the phasor diagram of Figure 2.2 represent the initial operating condition (with a Thevenin impedance of X_2) and the continuous line a new operating condition with a larger Thevenin impedance ($X_2^{(1)}$).

In both cases the system reactive power requirements are equally shared between the converter and the ac source with the same firing-angle used in both converter groups.

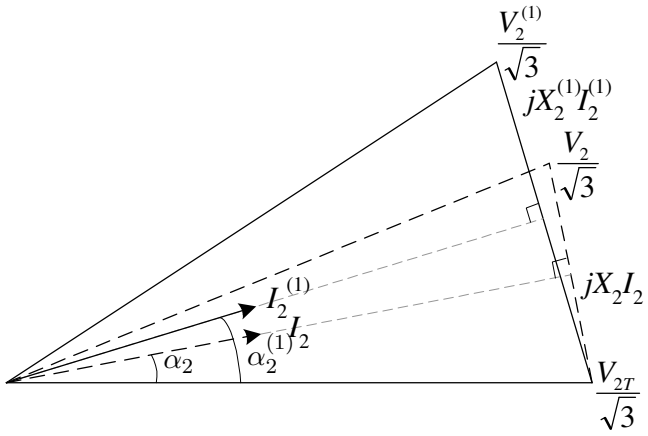


Figure 2.2 Operating conditions at the receiving end for two different system strengths

The condition is represented by the following equations:

$$I_{2A} = I_{2B} = k_m I_d \tag{2.1}$$

or between the double converter ac and dc currents

$I_2 = 2k_m I_d$ (where k_m=1.59)

and

$$\left(\frac{V_2}{\sqrt{3}}\right)^2 - \left(\frac{V_{2_T}}{\sqrt{3}}\right)^2 = X_2^2 I_2^2 - 2\left(\frac{V_{2_T}}{\sqrt{3}}\right) XI\sin(\alpha_2) \tag{2.2}$$

$$V_{d2} = 4(\frac{3\sqrt{2}}{\pi})V_{2T}\cos(\alpha_2) \tag{2.3}$$

In terms of the specified power (which is normally controlled at the sending end) the dc voltages across the link are related by the expression

$$V_{d1} = V_{d2} + R_d\frac{P_{d1}^{sp}}{V_{d1}}$$

Or, making V_{d1} the subject and taking the positive root:

$$V_{d1} = \frac{V_{d2} + \sqrt{V_{d2}^2 + 4R_d P_{d1}^{sp}}}{2} \tag{2.4}$$

The solution of equations (2.1) to (2.4) provides the initial values of α_2, V_{d2}, V_{d1} and I_2.

Sending end:

Figure 2.3 illustrates the two operating conditions in response to the change at the receiving end.

Initially the sending end is set with one firing-angle positive and one negative to demonstrate the phase-shift control principle, these are represented by α_{1A} and α_{1B}. When a change in operating conditions occurs, as a result of an increased Thevenin impedance and thus, of firing-angle at the receiving end, the sending end must compensate by an increase in firing-angle ($\alpha_{1A}^{(1)}$ and $\alpha_{1B}^{(1)}$ in Figure 2.3) to maintain the specified active power transfer.

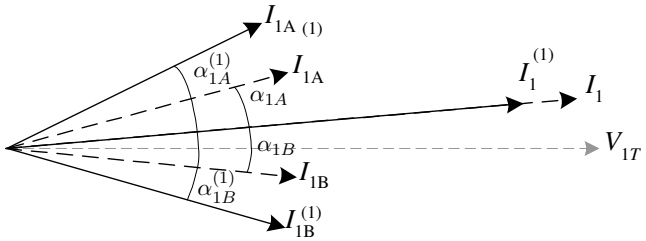


Figure 2.3 Firing-shift control maintaining constant reactive power at the sending end for two different system strengths

The following relationships apply to the sending end

$$V_{d1} = 2(3\frac{\sqrt{2}}{\pi})V_{1T}(\cos(\alpha_{1A}) + \cos(\alpha_{1B})) \tag{2.5}$$

$$I_{1A} = k_m I_d \tag{2.6}$$

and

$$I_1 = \sqrt{(I_{1A}\cos(\alpha_{1A}) + I_{1B}\cos(\alpha_{1B}))^2 + (I_{1A}\sin\alpha_{1A}) + I_{1B}\sin(\alpha_{1B}))^2}$$

or, because $|I_{1A}| = |I_{1B}|$ due to the series connection

$$I_1 = \sqrt{2}I_{1A}\sqrt{1+\cos(\alpha_{1A}-\alpha_{1B})} = 2I_{1A}\cos\left(\frac{(\alpha_{1A}-\alpha_{1B})}{2}\right) \tag{2.7}$$

The active power P_1 is equal to the specified dc powerP_{d1}^{sp}

$$P_1 = V_{1T}I_{1A}(\cos(\alpha_{1A}) + \cos(\alpha_{1B})) \tag{2.8}$$

and the reactive power

$$Q_1 = V_{1T}I_{1A}(\sin(\alpha_{1A}) + \sin(\alpha_{1B})) \tag{2.9}$$

With V_1, V_{1T} and P_1 specified, the unknown variables are V_{d1}, I_{1A}, I_1, α_{1A}, α_{1B} and Q_1, which can be derived from the simultaneous solution of equations (2.4) to (2.9).

In the steady state, the values of α_{1A} and α_{1B}, and thus the internal reactive power circulation between the two converter groups, can be reduced by the use of transformer on load tap change.

2.4 CONTROL STRUCTURE

For complete flexibility the sending end needs to control real and reactive power and the receiving end keep the converter dc voltage constant (so as to minimise dc current for a given real power setting) and control the reactive power. With reactive power control at both ends, the controllers can easily be configured for optimum power transfer at the system level depending on operating objectives, which usually involves providing constant power factor at the sending end and constant AC terminal voltage at the receiving end.

In order to control the real and reactive power over the complete operating range the converter response needs to be linear. Standard PID controllers are unsuitable for this application as their gain is static, and although they may give suitable performance over a narrow band, the latter is not acceptable over the complete range. This is explained in more detail later.

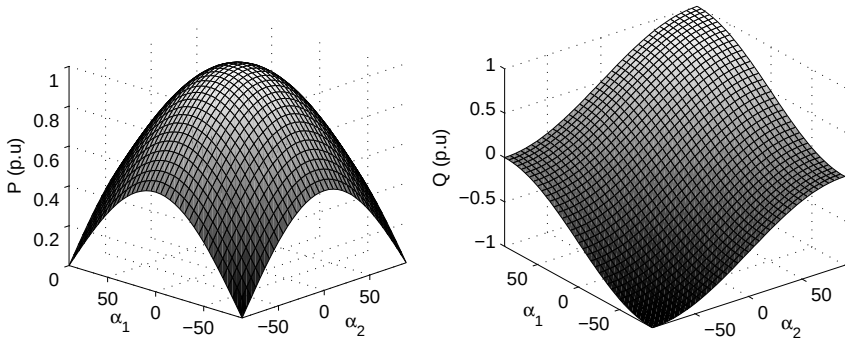


Figure 2.4 Calculated real and reactive power for varied firing-angle (±90°)

Figure 2.4 illustrates the control ranges of the real and reactive power responses for α values of ±90°. It is clear that these controller surfaces are very non linear, and it is not hard to understand why a linear PID controller would be unsuitable.

Given the above controller surfaces, it is difficult to visualise how the controller must perform, especially since the controller firing-angles are expected to operate equally well in the positive and negative regions. What is needed is a controller that operates for all combinations of P and Q without the need to manually switch controller gains and control actions. An example of four controller operating conditions is shown in Figure 2.5.

These diagrams show that the controller is expected to operate over a wide range of conditions and that the change in firing-angle has the greatest influence on the real power near the X axis and on the reactive power near the Y axis. This is better explained by examining the real and reactive power contribution of one converter in isolation. The real power transferred by the converter depends on the cosine of the firing angle α_1 while the reactive power depends on the sine of α_1. What is of interest to control system designers is the rate of change of the controlled

outputs P and Q,as this determines the level of gain (or sensitivity) in system response. Basic differentiation reveals that the rate of change is proportional to $-\sin(\alpha_1)$ for real power and to $\cos(\alpha_1)$ for reactive power, which makes this system very non-linear.

As mentioned earlier, conventional controller operation is confined to a relatively small range and functions with a fixed gain, thereby assuming that the system is linear over the small range. This control philosophy becomes even less suitable when we consider that an ideal independent and fully flexible controller should be able to provide a combination of α_1 and α_2 that satisfies the requirements of both P and Q simultaneously.

Figure 2.6 illustrates a simplified block diagram of what the controller must achieve, the goal being a mapping function that translates P and Q into α_1 and α_2, to make the nonlinear converter appear linear.

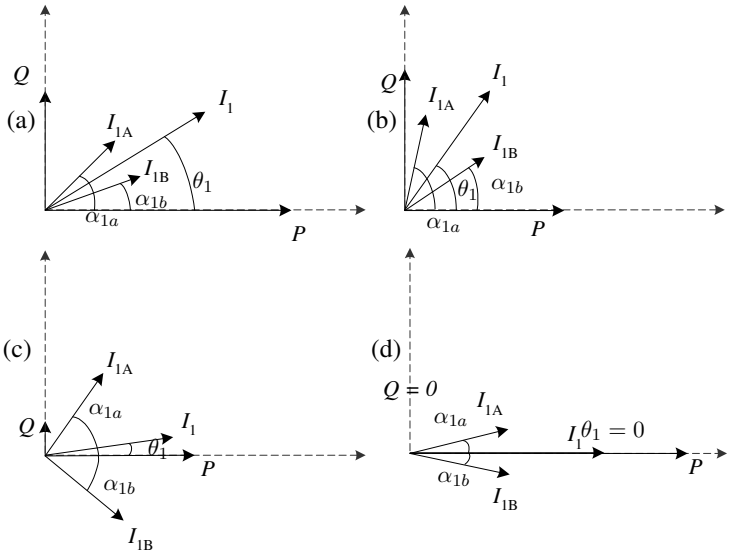


Figure 2.5 Firing-shift control providing (a) Large P and Q, (b) Large Q & smaller P, (c) Small P & Q, and (d) Large P, no Q

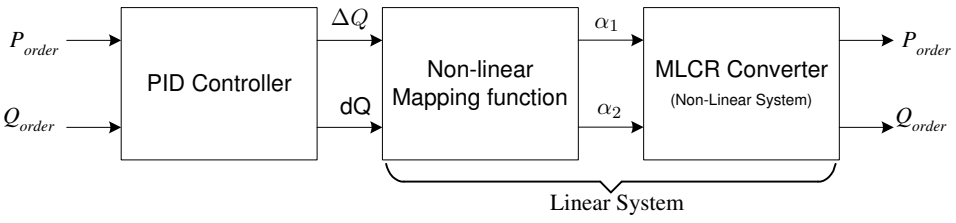


Figure 2.6 Block diagram of Non linear system control objective

The only information representing the behaviour of the converter system is given by the equations (2.8) and (2.9), but this is sufficient initially, because they show the influence that $\Delta\alpha_1$ and $\Delta\alpha_2$ have on the output variables P and Q.

The rate of change of the output variables with respect to firing-angles α_1 and α_2 can be expressed as:

$$\Delta P = \frac{\partial P}{\partial \alpha_1}\Delta\alpha_1 + \frac{\partial P}{\partial \alpha_2}\Delta\alpha_2 \tag{2.10}$$

$$\Delta Q = \frac{\partial Q}{\partial \alpha_1}\Delta\alpha_1 + \frac{\partial Q}{\partial \alpha_2}\Delta\alpha_2 \tag{2.11}$$

These are found by differentiating the equations (2.8) and (2.9), i.e.

$$\frac{\partial \mathrm{P}}{\partial \alpha_1} = -3V_T I_1 \sin(\alpha_1) \tag{2.12}$$

$$\frac{\partial \mathrm{P}}{\partial \alpha_2} = -3V_T I_1 \sin(\alpha_2) \tag{2.13}$$

$$\frac{\partial \mathrm{Q}}{\partial \alpha_1} = 3V_T I_1 \cos(\alpha_1) \tag{2.14}$$

$$\frac{\partial \mathrm{Q}}{\partial \alpha_2} = 3V_T I_1 \cos(\alpha_2) \tag{2.15}$$

Expressing the dynamic system in matrix form

$$\begin{bmatrix} \Delta P \\ \Delta Q \end{bmatrix} = \underbrace{\begin{bmatrix} \frac{\partial \mathrm{P}}{\partial \alpha_1} & \frac{\partial \mathrm{P}}{\partial \alpha_2} \\ \frac{\partial \mathrm{Q}}{\partial \alpha_1} & \frac{\partial Q}{\partial \alpha_2} \end{bmatrix}}_{A} \begin{bmatrix} \Delta\alpha_1 \\ \Delta\alpha_2 \end{bmatrix} \tag{2.16}$$

Equation (2.16) can be solved using basic matrix theory.

Using the partial differentials of the equations to P and Q in Matrix A, it is possible to model the converter systems transient response (but not the system state).

If the matrix is non singular, its inverse can be used to linearise the converter system behaviour. The inverse of Matrix A, with the common gain component grouped on the left side, becomes:

$$A^{-1} = \frac{1}{3V_T I_1 \sin(\alpha_1 - \alpha_2)} \begin{bmatrix} -\cos(\alpha_2) & -\sin(\alpha_2) \\ \cos(\alpha_1) & \sin(\alpha_1) \end{bmatrix} \tag{2.17}$$

This equation indicates that the overall system gain depends on the difference between the two firing-angles ($\sin(\alpha_1$- $\alpha_2)$) and the contribution of (for P) real power on the other groups firing-angle, and (for Q) reactive power contribution on the other groups firing-angle. While making sense in theory, this needs to be realised in practice.

Examining the system on an incremental basis (i.e. from α_1 to α_1+ $\delta\alpha_1$), as the difference ($\delta\alpha_1$) is reduced the accuracy is increased, becoming very close to the continuous integral equivalent. It could be argued that in each partial differential equation the effect of $\Delta\alpha_1$ on $\Delta\alpha_2$ and vice

versa is not fully captured, but in a practical system this effect can be minimised with suitable feedback

2.4.1 Practical Implementation

Figures 2.7 and 2.8 show the implementation of the theory into a real system controller.

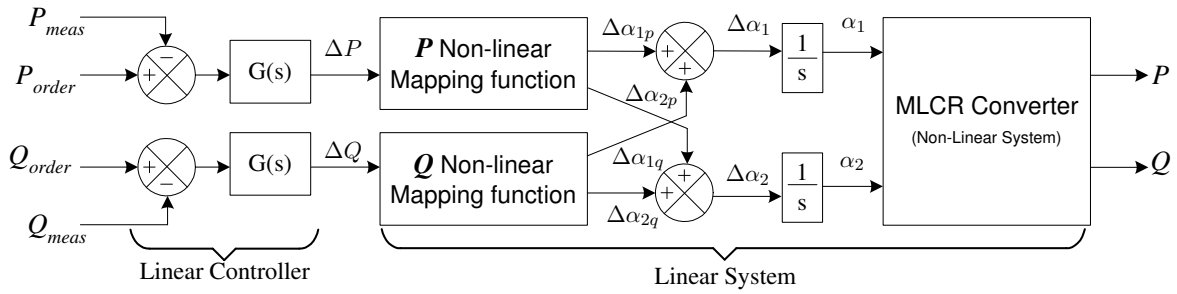


Figure 2.7 Implementation of Non-linear control theory

In Figure 2.7, the controller has 2 separate channels, one for each of the P and Q components. For each channel, the theory is the same; the error is calculated by subtracting the measured power from the power order, and this is fed into the PID controller. The increment of ΔP and ΔQ becomes the input into the non-linear mapping function, which resolves the increment of ($\Delta\alpha_{1P}$ & $\Delta\alpha_{2P}$), and ($\Delta\alpha_{1Q}$ & $\Delta\alpha_{2Q}$) from the P and Q channels respectively. The non linear errors are combined and then $\Delta\alpha_1$ & $\Delta\alpha_2$ are integrated to provide the required outputs (α_1) & (α_2) as inputs into the converter firing logic.

The non Linear mapping function in Figure 2.7 for P is represented byA_{11}^{-1}, A_{21}^{-1} , and for Q is A_{12}^{-1}, A_{22}^{-1} in (2.17).

Figure 2.8(a) shows how the system is realised in a practical controller. The controller layout follows almost exactly the analytical development from (2.10) to (2.17), with only additional low pass filters added to prevent ringing when the error is almost zero. It is important to note that the common component of the converter control is calculated separately (Figure 2.8(b)), as this determines the overall gain of the system. Hard limits on the calculation are provided so as to prevent wind up and instability which can occur if $\alpha_1 = \alpha_2$. Also to ensure that firing-angle α_1 is always greater than α_2, limits are placed on the integrators.

The receiving end controller topology is much the same as that of the sending end, but as it must control V_{d_r} and Q_r, the layout is different. Using equations (2.5) and (2.9), the inverse transfer function becomes:

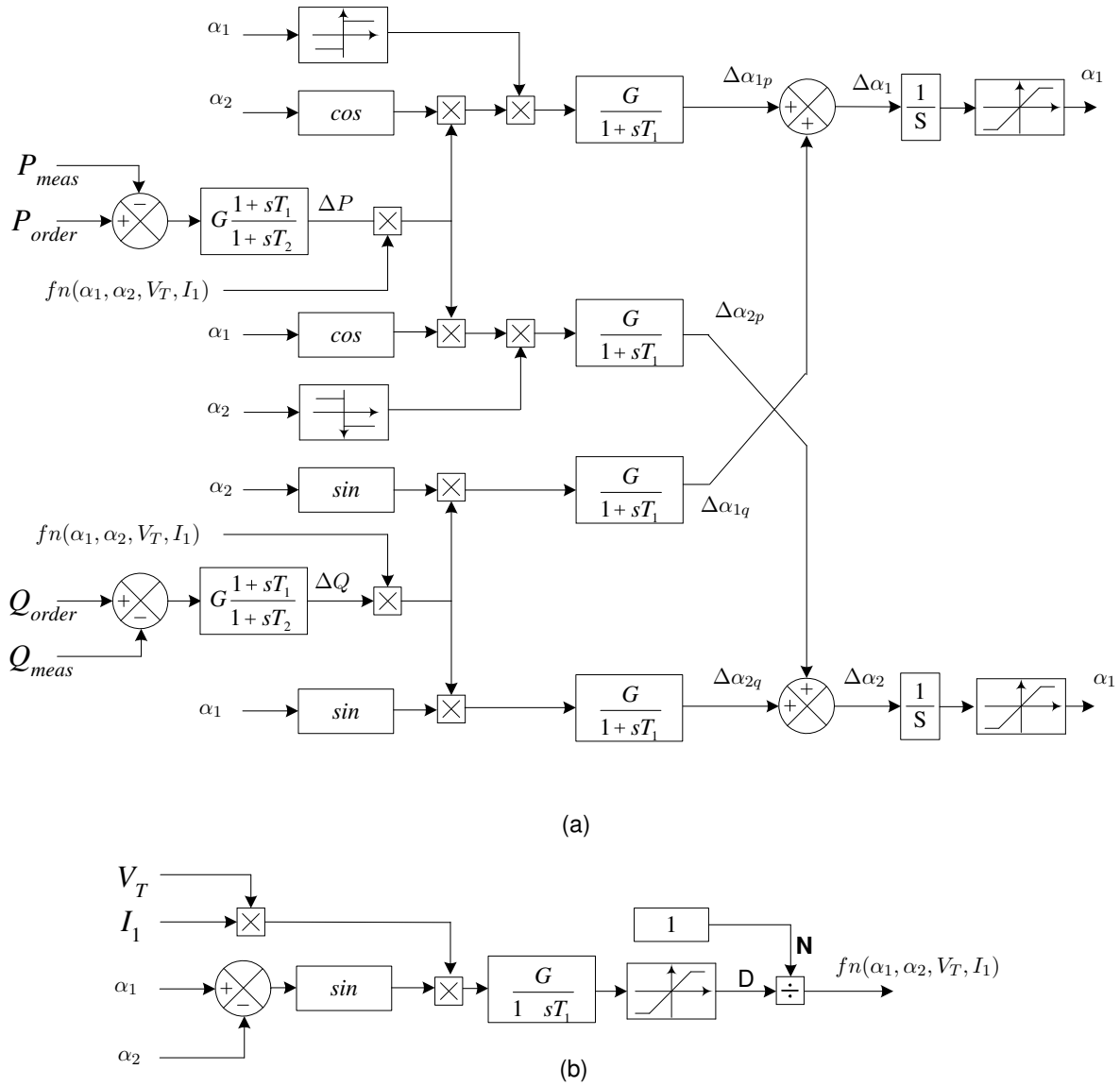


Figure 2.8 Sending end controller block diagram, with the main linearising components in (a) and the common angle difference calculation in (b)

$$A^{-1} = \frac{1}{3V_T \sin(\alpha_1 - \alpha_2)} \begin{bmatrix} \frac{-\sqrt{2}\pi\cos(\alpha_2)}{4} & \frac{-\sin(\alpha_2)}{I_1} \\ \frac{\sqrt{2}\pi\cos(\alpha_1)}{4} & \frac{\sin(\alpha_1)}{I_1} \end{bmatrix} \tag{2.18}$$

Given these equations and taking into consideration (2.6) it becomes apparent that although full control is justified by the theory, the range of Q control depends on the magnitude of I_d. Optimum dc power transmission occurs when the dc current is minimised, as this also minimises the dc link power losses; however this affects the range of Q controllability at both the sending and receiving ends. As the reactive power circulation is confined to the AC system side, the magnitude of the ac current in each converter group determines the level of reactive power

controllability in the AC system. The real power, which is also a function of the AC current magnitude, is determined by the combination of V_d and I_d on the dc link. To understand the reactive power controllability limits, it must be realised that the same amount of real power can be transferred with a combination of high V_d/low I_d, or low V_d/high I_d.

An example of this in a multi-group MLCR, in per unit terms is given below:

$$\text{High } V_d : P_d = 1pu = 5.5puV_d \times 0.182puI_d \tag{2.19}$$

$$\text{Low } V_d : P_d = 1pu = 2.25puV_d \times 0.364puI_d \tag{2.20}$$

and so with $I_1 = \sqrt{3}k_m I_d$ and V_{ac} being the same in both cases, equation (2.9) shows that equation (2.19) would yield twice the reactive power for a given firing-angle as (2.20).

So with conflicting objectives in real power efficiency and reactive power controllability, a compromise must be made between control range and overall efficiency during system design.

2.5 DYNAMIC SIMULATION

2.5.1 Test System

The test circuit is a simplified HVDC link configuration with the two interconnected systems represented as Thevenin equivalents. As shown in Figure 2.1, each terminal consists of two five-level MLCR converter groups.

Using 1000 MW and 220 kV as base values, the source voltages are set at 1.06 and 1.02pu at the sending and receiving ends respectively. The series impedances at the sending and receiving ends are set to 0.2pu to represent systems with SCRs of approximately 3, and the transformer leakage reactance of all converter transformers is equal to 0.1 pu. The dc line is represented by a resistance of 0.2 pu in series with a 2 H smoothing inductor. The active power transfer and reactive power are the controlled variables at the sending end; at the receiving end the controlled variables are the dc voltage and the reactive power order.

2.5.2 Simulation Verification and Reactive power independence

The test system has been modelled using the PSCAD/EMTDC package and the response to a series of step changes over a 3 second period are presented in Figure 2.9.

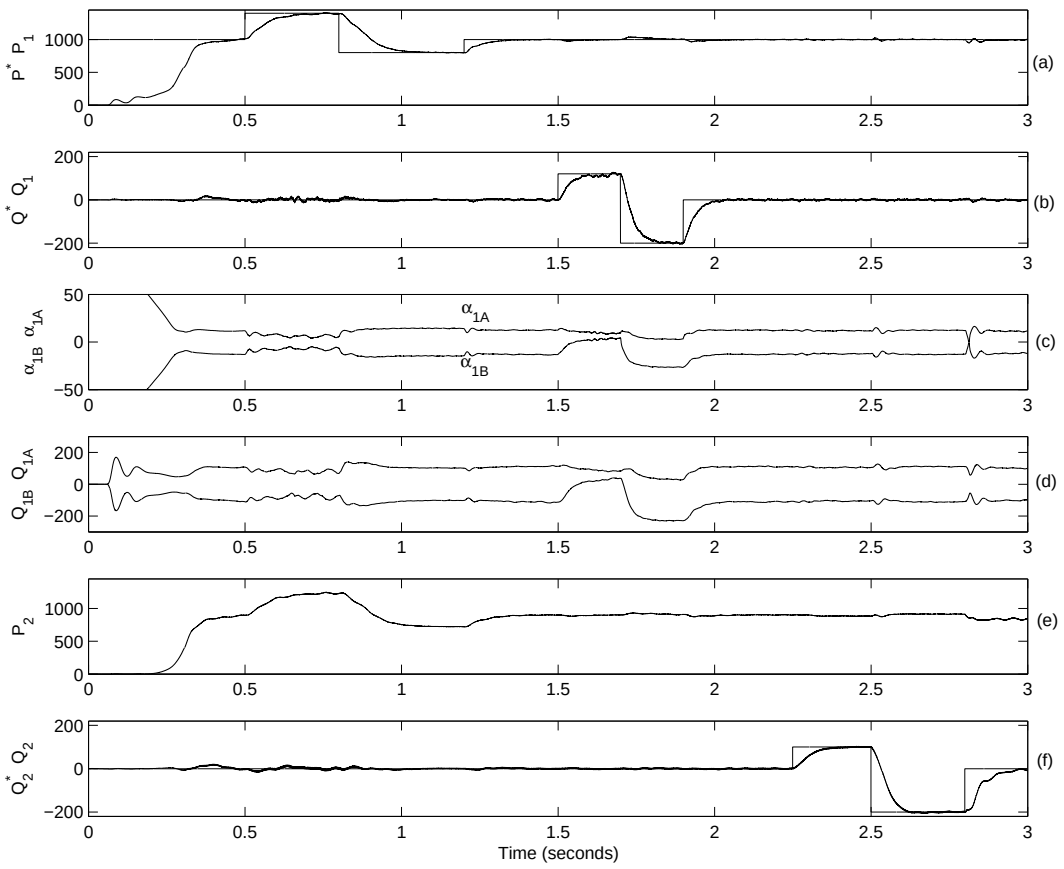


Figure 2.9 Real and reactive power order changes at the sending and receiving ends

Changes in the active power order from 1000 to 1400 MW (at 0.5s) and from 1400 to 800 MW (at 0.75s) are shown in Figure 2.9(a); their effect on the reactive power at either end of the link is shown in graphs (b) and (f) to be negligible.

Likewise, Figure 2.9(b) shows step changes in the reactive power order at the sending end, first from 0 to +100 MVAr (at 1.5s) and later from +100 to -200 MVAr (at 1.7s); the effect on the receiving end active and reactive power (shown in graphs (e) and (f) respectively) are also negligible and they only cause a slight disturbance to the active power at the sending end (as shown in graph (a)).

The effect of the above changes on the group firings at the sending end, illustrated in graph (c), show that α_{1B} can operate with positive and negative values, thereby minimising the reactive power circulation between the groups (clearly noticeable between 1.5 and 1.7 s in graph (d)). Figure 2.9(f) shows a change in the reactive power order at the receiving end, from 0 to 100 MVAr (at 2.25s) and from 100 to -200 MVAr (at 2.5s). These produce a small change of active power, which requires a small correction in the firing-angle, but no visible change is observed in the sending end reactive power (graph (b)).

As the secondary control objective is to maintain dc voltage constant, a maximum step of +100 MVAr is possible at the receiving end. This is because the receiving end terminal voltage decreases as more reactive power is required by the converter, which further contributes to the decrease in dc voltage for a given firing-angle.

2.5.3 Simulation of unity power factor and constant terminal voltage operation

The dynamic simulation in PSCAD/EMTDC features the effect of four separate controllers, one for each of the reactive powers, and one for the sending end real power and receiving end dc voltage. By adding an extra controller to each of the reactive power orders, it is possible to control the system to provide unity power factor and constant terminal voltage over the complete real power operating range.

The sending end correction is made from the point of view of the AC system, so the converter controller is configured to maintain the power factor of the main supply transmission line as well. In practice it may not be possible to calculate the impedance of the supply in all cases, and an approximation would have to be made about a nominal correction point.

At the receiving end, the control of the terminal voltage should be easier to achieve, as the nominal supply voltage would be known, or could be calculated. This could also be adjusted manually by the system operator to provide additional voltage support as necessary.

Figure 2.10 (a – f) presents an example of the multi group MLCR dc link providing power factor correction and terminal voltage control. To highlight the dynamics of the control method, the real power order is modified in (a) in a series of steps, as listed in Table 2.1.

Table 2.1 Summary of step changes for simulation in Figure 2.9

time(s)	0.0	1.0	1.5	2.0	2.5	3.0	3.5	4.0	4.5
$P_{Send}(MW)$	100	250	500	750	1000	750	500	250	0

The reactive power responses are plotted in Figure 2.10(b) & (e) for the sending and receiving ends respectively and the sending end power factor in (c). In (f) the constant line represents the receiving end source, and the second line the terminal voltage.

It is important to note in (e) and (f), that under this control scheme (i.e. with optimised V_d) for real power transfers of 250 and 500 MW, the ac current at the receiving end is insufficient to provide stable terminal voltage control. This highlights one of the limitations of maximising V_d; although however, this can be easily corrected by reducing V_d during situations where low real power transfer is required.

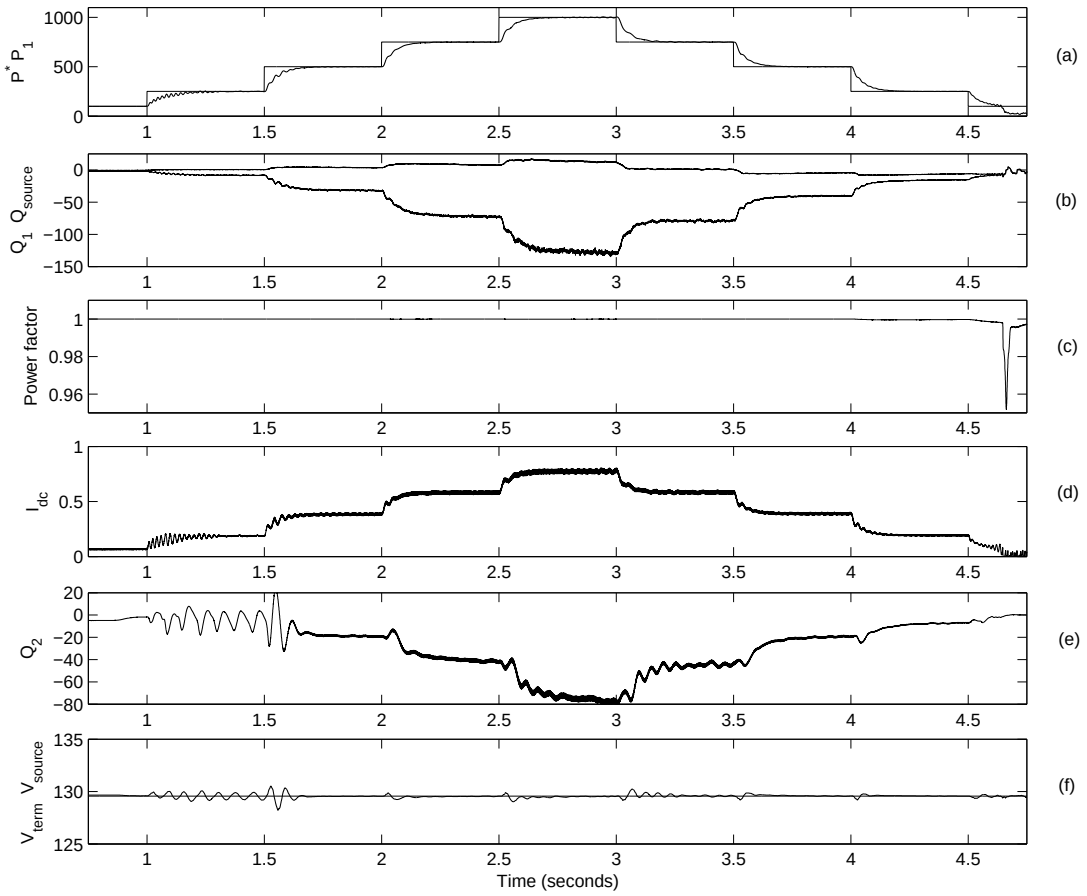


Figure 2.10 Reactive power responses under power factor and terminal voltage control for a series of step changes to real power

2.6 CONCLUSIONS

A new type of converter control has been developed, applicable to multi-level HVDC schemes with two or more twelve-pulse groups per terminal. It has been shown theoretically, and verified by EMTDC simulation using an MLCR configuration, that the use of a controllable shift between the firings of the series-connected converter groups permits independent reactive power control at the two dc link terminals. This provides four quadrant power controllability to multi-level current source HVDC Transmission and, thus, makes this alternative equally flexible to PWM-controlled Voltage Source Conversion, without the latter's limitations in terms of power and voltage ratings. It can be expected that MLCR combined with firing-shift control should compete favourably with the conventional current source technology for very large power applications.

Chapter 3

FLEXIBLE BACK-TO-BACK POWER CONVERSION FOR LARGE POWER SYSTEM INTERCONNECTIONS

3.1 INTRODUCTION

Driven mainly by cost and switching efficiency, the large power DC interconnections are still based on conventional thyristor conversion, which is very limited in terms of control flexibility. This also applies to Back to Back asynchronous interconnections, some of which have already reached the 1500MW mark, for the interconnection of networks of different frequencies [28], for trading reserves [29] and to shift peak energy loading times between networks with different time zones [30].

As the rating and acceptability of high power self-commutating switches improve, the boundaries between the HVDC and FACTS technologies are gradually becoming blurred. HVDC is beginning to use the new devices (and thus improve its control flexibility) and FACTS devices are increasing their power range, which may finally result in the control of the total power transfer in asynchronous interconnections. Therefore, modern back to back (BTB) conversion can be considered as part of the HVDC and FACTS technologies.

The distinguishing feature of FACTS with respect to traditional HVDC has been control flexibility, which, until recently, has been the privilege of the FACTS technology. However, several fully flexible PWM-based HVDC Voltage Source Conversion distance schemes in the 300MW region are now operating successfully and the power rating capability of the PWM-VSC technology is on the increase.

Proposals have also been made to introduce multi-level self-commutating conversion with increased active and reactive power controllability. However, apart from their structural complexity, when applied to DC transmission the multi-level alternatives still lack independence of reactive power controllability between the two ends of the link. This is an important limitation for the exchange of large power transfer, particularly between relatively weak systems.

The Multi-Level Current Reinjection (MLCR) scheme using parallel connected bridges [31] is a

structurally simpler conversion alternative to the conventional Multi-Level configurations. While attractive for industry application, this alternative is not practical for long distance HVDC transmission, that requires the use of series connected bridges.

However, the high power ratings of some modern BTB interconnections will normally consist of series/parallel combinations of converter bridges because, unlike long distance HVDC, the absence of transmission distance in the BTB case justifies relatively lower voltages and higher currents. Moreover, the previous chapter has shown that the problem of reactive power interdependence between the two ends of the link, inherent in all multi-level configurations, can be solved when the power rating justifies the use of multi-group conversion, by means of phase-shifting control of the groups firings. The added control flexibility and high-pulse operation eliminates the need for shunt reactive power compensation and harmonic filters, and thus presents a potential cost advantage over an equivalent Line commutated conversion (LCC) scheme.

This chapter summarises the development of a 4-quadrant series-parallel BTB configuration based on the MLCR parallel converter. The configuration takes advantage of these two advances in converter control flexibility to provide the most economical combination of the voltage and current levels. The theory is verified by EMTDC simulation.

3.2 PROVISION OF INDEPENDENT REACTIVE POWER CONTROLLABILITY

Figure 3.1 presents a series-parallel connected back to back link, interconnecting two separate ac systems represented by Thevenin equivalents V_s, Z_s and V_r, Z_r respectively.

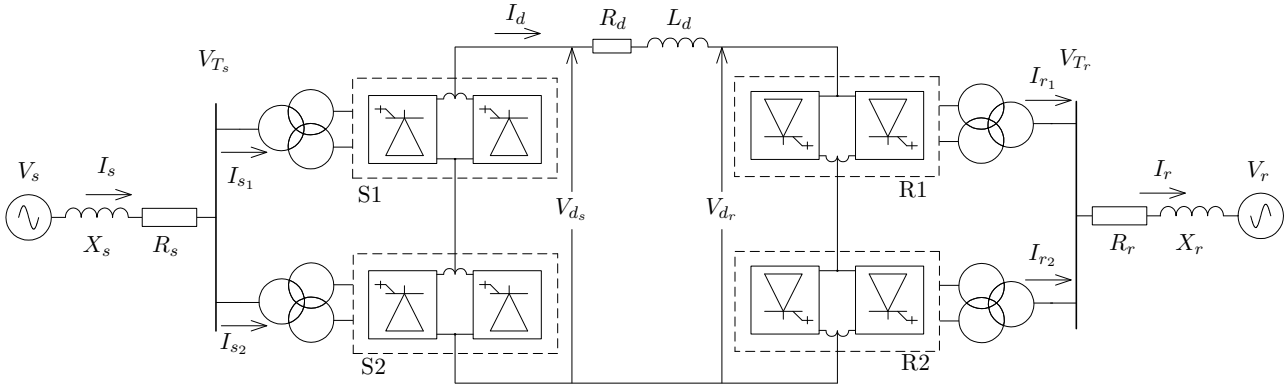


Figure 3.1 Block diagram of the back to back link configuration

The converters at the sending end (denoted by $_s$) are parallel connected on their respective ac sides with a common terminal voltage (V_{T_s}) and series/parallel connected on the dc side with a combined dc voltage (V_{d_s}). The difference between V_{d_s} and the receiving end dc voltage (V_{d_r}) over the dc side resistance (R_d) determines the resulting dc current which is then inverted at the receiving end.

For the series connected ac-dc rectifiers, the combined dc voltage at the sending end is

$$V_{d_s} = k_1 V_{T_s} \cos(\alpha_{s_1}) + k_1 V_{T_s} \cos(\alpha_{s_2}) \tag{3.1}$$

where k_1 is a constant that depends on the converter topology and α_{s1} and α_{s2} are firing-angles, which under self-commutation are considered to be capable of leading or lagging the terminal voltage reference.

The reactive power of rectifier S1 is given by

$$Q_{T_{s1}} = 3V_{T_s} k_2 I_d \sin(\alpha_{s_1}) \tag{3.2}$$

where I_d is the dc current and k_2 is the ac rms fundamental to dc current ratio that depends on the number of levels. For a 5-level MLCR, $k_2 \simeq 0.8$ [31]. For negative values of α_{s_1} relative to the voltage V_{T_s}, reactive power is generated and supports the terminal voltage V_{T_s}. The net reactive power generated or absorbed by the series connected sending end rectifiers (at the common terminal) is therefore

$$\begin{aligned} Q_{T_s} &= 3V_{T_s} k_2 I_d \sin(\alpha_{s_1}) + 3V_{T_s} k_2 I_d \sin(\alpha_{s_2}) \\ &= 3V_{T_s} k_2 I_d (\sin(\alpha_{s_1}) + \sin(\alpha_{s_2})) \end{aligned} \tag{3.3}$$

By selecting suitable values of α_{s_1} and α_{s_2} in (3.3), the reactive power demands may be controlled. Moreover, by specifying firing-angles that satisfy *both* equations (3.1) and (3.3), the dc voltage and reactive power at the sending end may be controlled simultaneously and independently, and on-load tap-changers can be eliminated.

If the transformer real power losses are neglected, the sending end terminal real power P_{T_s} is given by

$$P_{T_s} = P_{d_s}(\text{dc power}) = V_{d_s} I_d \tag{3.4}$$

and substituting equation (3.1) into (3.4), the relationship is thus

$$P_{T_s} = 3k_1 V_{T_s} I_d (\cos(\alpha_{s_1}) + \cos(\alpha_{s_2})) \tag{3.5}$$

The RMS ac supply current I_s is related to the dc current by

$$I_s = 2k_2 I_d \cos\left(\frac{\alpha_{s_1} - \alpha_{s_2}}{2}\right) \tag{3.6}$$

the magnitude and phase of supply current (I_s) through the system impedance (Z_s) determining the voltage V_{T_s} for a active power flow. By combining (3.6) with (3.3) and (3.5), the sending end terminal active and reactive powers (P_{T_s} and Q_{T_s}) may therefore be rewritten as

$$P_{T_s} = 3\frac{k_1}{k_2}V_{T_s}I_s\cos\left(\frac{\alpha_{s_1}+\alpha_{s_2}}{2}\right) \tag{3.7}$$

and

$$Q_{T_s} = 3\frac{k_1}{k_2}V_{T_s}I_s\sin\left(\frac{\alpha_{s_1}+\alpha_{s_2}}{2}\right) \tag{3.8}$$

From (3.4), the dc power transfer may be achieved with any combination of V_d and I_d that satisfies a constant P_T. Unlike with HVDC transmission, where V_{d_s} is maximised to reduce transmission losses, the back to back link dc losses are negligible, and freedom exists to control the dc current across its full range. The level of reactive power controllability (from (3.3)), at both the sending and receiving ends, depends on the magnitude of the dc current, and so for a given real power transfer, increasing I_d is of real benefit when the converter interconnects two weak systems.

The converter ends are identical and so equations (3.1) to (3.8) are modified for the receiving end by replacing the subscript ($_s$) with ($_r$). The receiving end dc voltage is thus described by:

$$V_{d_r} = k_1V_{T_r}(\cos(\alpha_{r_1}) + \cos(\alpha_{r_2})) \tag{3.9}$$

If the active power transfer across the back to back link is specified at the sending end, then the level of dc current may be modulated by adjusting the receiving end dc voltage; i.e. the dc current is increased by driving V_{d_r} down relative to V_{d_s} as given by

$$I_d = \frac{V_{d_s} - V_{d_r}}{R_d} \tag{3.10}$$

In practice the BTB link resistance is negligible, meaning that the sending and receiving end voltage are almost the same. The resistance has been introduced to illustrate the how the dc current may be adjusted. There will however, be instantaneous differences in voltage across the smoothing reactor L_d.

Decreasing the receiving end dc voltage to increase the dc current has an immediate effect on the sending end power and, as a consequence, the sending end dc voltage must be reduced to maintain the specified power. Therefore in terms of specified dc real power ($P_{d_{ref}}$), receiving end dc voltage (V_{d_r}) and dc resistance (R_d),

$$V_{d_s} = \frac{V_{d_r} + \sqrt{V_{d_r}^2 + 4R_dP_{d_{ref}}}}{2} \tag{3.11}$$

The flexibility in dc voltage and current in a back to back configuration also permits large dc current at low real power settings, meaning that reactive power compensation is possible at both ends of the link, even when real power transfer is not required.

3.3 MLCR BACK TO BACK LINK

The MLCR topology, developed in both series and parallel configurations [31, 32], has high pulse capability and operates with either a leading or lagging firing-angle, whilst retaining conventional thyristor (SCR) main bridges. In back to back HVDC conversion, dc losses are negligible and a relatively low dc voltage permits positioning of converters in close proximity, which results in a smaller overall station footprint. With higher current for a specified active power transfer as compared to long distance HVDC transmission, the parallel MLCR converter (summarised in Appendix B) is better suited as it has fewer switches in the conduction path than its series counterpart, and therefore lower comparative losses.

Owing to the near sinusoidal MLCR supply current, a small voltage phase-shift across the transformer leakage reactance occurs under load, which depends on the converter firing-angle. The phase-shift is neglected in conventional LCC because minimum firing-angle is generally greater than 10°, but must be considered in 4 quadrant operation as the converter control action changes depending on operating quadrant. This effect is shown for the sending end in Figure 3.2, where $V_{T_{s1}}$ and $V_{T_{s2}}$ are the voltages on the converter side of the transformers.

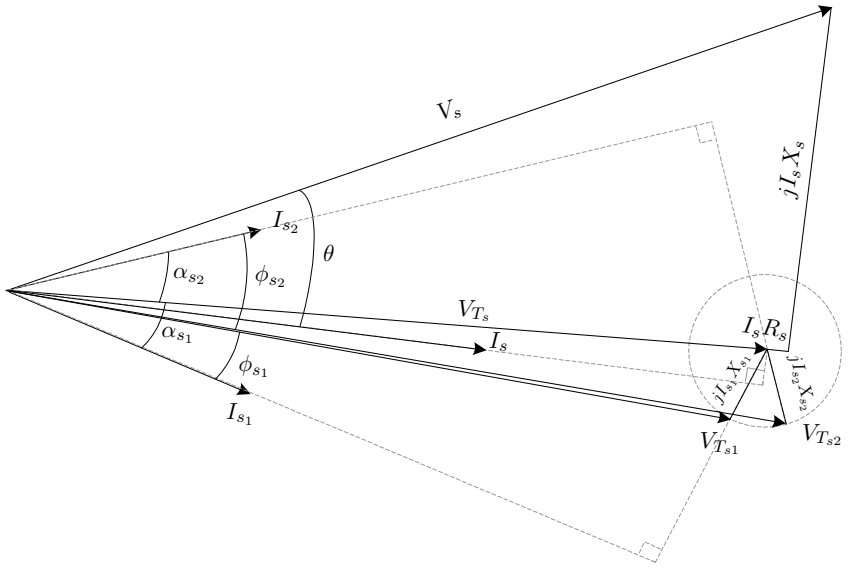


Figure 3.2 Phasor diagram of the phase-shift across system impedance and transformer leakage reactances at the sending end of a series connected parallel-MLCR converter

The locus centred about the peak of V_{T_s} describes the phase-shift caused by the transformer leakage reactances $jI_{s_1}X_{s_1}$ and $jI_{s_2}X_{s_2}$ for a given dc current (as $|I_{s_1}| = |I_{s_2}| = k_2 I_d$). The

specified firing-angles (α_{s_1} and α_{s_2} in the diagram) referenced to common terminal voltage V_T actually result in angles which differ slightly relative to their individual terminal voltages, as denoted by ϕ_{s_1} and ϕ_{s_2}. Firing-angle is therefore determined with reference to the converter transformer secondary side voltages $V_{T_{s1}}$ and $V_{T_{s2}}$.

3.3.1 Determining the dc voltage operating limits

The firing-angle limits at both converter ends are set by the active and reactive power requirements. The minimum and maximum values of the sending end system impedance define the limits of reactive power generation required by the rectifier to maintain the ac terminal voltage at rated active power transfer. In terms of the specified dc power ($P_{T_{ref}}$), equations (3.1) and (3.3) may be expressed as

$$\begin{aligned} Q_{T_s} &= 3V_{T_s}I_{s_1}(\sin(\alpha_{s_1}) + \sin(\alpha_{s_2})) \\ &= 3V_{T_s}k_2I_d(\sin(\alpha_{s_1}) + \sin(\alpha_{s_2})) \\ &= 3V_{T_s}\frac{k_2P_{T_{ref}}}{V_d}(\sin(\alpha_{s_1}) + \sin(\alpha_{s_2})) \end{aligned} \tag{3.12}$$

or

$$\begin{aligned} Q_{T_s} &= \frac{3k_2P_{T_{ref}}(\sin(\alpha_{s_1}) + \sin(\alpha_{s_2}))}{k_1(\cos(\alpha_{s_1}) + \cos(\alpha_{s_2}))} \\ &= \frac{3k_2P_{T_{ref}}}{k_1}\tan\left(\frac{\alpha_{s_1} + \alpha_{s_2}}{2}\right) \end{aligned} \tag{3.13}$$

Rearranging to make α_{s_2} the subject,

$$\alpha_{s_2} = 2\arctan\left(\frac{Q_Tk_1}{3k_2P_{T_{ref}}}\right) - \alpha_{s_1} \tag{3.14}$$

By substituting values of α_{s_1} such that $-90 \leq (\alpha_{s_1}$ and $\alpha_{s_2}) \leq 90$ the valid range of dc voltages can be determined.

An example of application is given in Figure 3.3 for an 1100 MW system with an SCR of 2 at both the sending and receiving ends to illustrate the dc side flexibility with constant ac conditions. The ac terminal voltage (V_{T_s}) at the sending end is maintained with 250 MVAr generated.

Figure 3.3(a) gives the dc voltage range where both active and reactive power can be delivered,

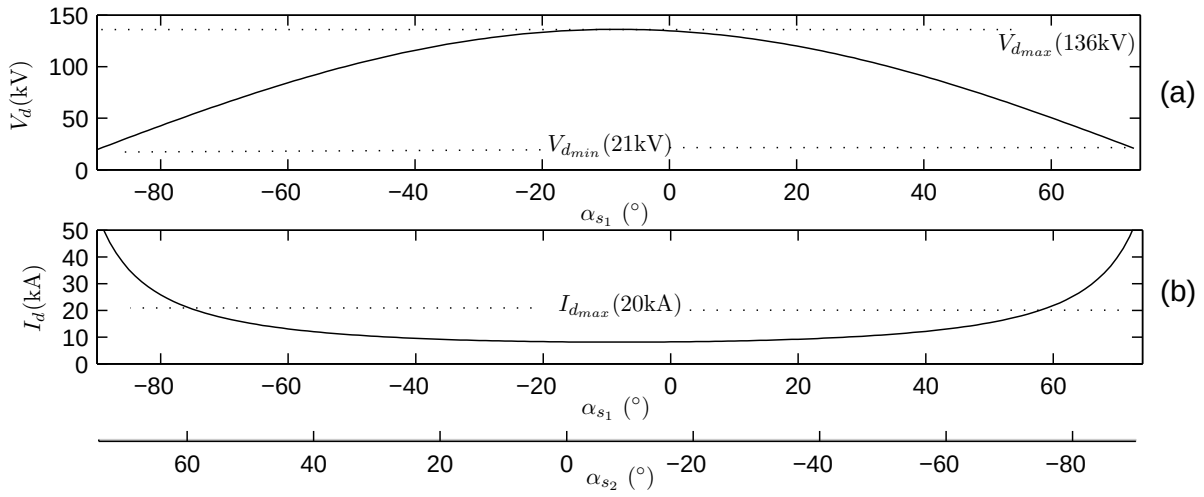


Figure 3.3 1100 MW BTB MLCR sending end dc characteristics while supplying 250 MVAr reactive power generation. With (a) dc voltage range and (b) dc current range

with minimum and maximum voltages indicated. Figure 3.3(b) gives the corresponding dc current range and dc limits, with an arbitrary dc side current rating of 20 kA indicated. This further refines the control range and increases the minimum dc voltage limit to $\simeq 55kV$.

3.4 CONTROL SYSTEM DESIGN

In order to control the terminal active and reactive power independently, the converter responses are linearised by taking the partial derivatives of (3.3) and (3.5) with respect to α_{s_1} and α_{s_2}, the inverse of which, in matrix form, is given as:

$$A_s^{-1} = \frac{1}{3V_{T_s}k_2I_d\sin(\alpha_{s_1}-\alpha_{s_2})}\begin{bmatrix} -\cos(\alpha_{s_2}) & -\sin(\alpha_{s_2}) \\ \cos(\alpha_{s_1}) & \sin(\alpha_{s_1}) \end{bmatrix} \tag{3.15}$$

and thus with

$$\begin{bmatrix} A_s^{-1} \end{bmatrix}\begin{bmatrix} \Delta P_{T_s} \\ \Delta Q_{T_s} \end{bmatrix} = \begin{bmatrix} \Delta\alpha_{s_1} \\ \Delta\alpha_{s_2} \end{bmatrix} \tag{3.16}$$

and P_{T_s} and Q_{T_s} specified, the increment in both firing-angles may be derived, without requiring the use of dc voltage as a control variable. In practice, when $\alpha_{s_1} = \alpha_{s_2}$ in (3.15), $\sin(\alpha_{s_1} - \alpha_{s_2})$ will be zero, with an undefined result, and so the denominator of (3.15) is limited to non-zero values to prevent control instability.

Similarly at the receiving end with the dc voltage and reactive power Q_{T_r} (and thus terminal voltage V_{T_r}) under control, the linearisation is performed by

$$A_r^{-1} = \frac{1}{3V_{T_r}\sin(\alpha_{1_r} - \alpha_{2_r})} \begin{bmatrix} \frac{-3\cos(\alpha_{r_2})}{k_1} & \frac{-\sin(\alpha_{r_2})}{k_2 I_d} \\ \frac{3\cos(\alpha_{r_1})}{k_1} & \frac{\sin(\alpha_{r_1})}{k_2 I_d} \end{bmatrix} \tag{3.17}$$

and similarly

$$\begin{bmatrix} A_r^{-1} \end{bmatrix} \begin{bmatrix} \Delta V_{T_r} \\ \Delta Q_{T_r} \end{bmatrix} = \begin{bmatrix} \Delta\alpha_{r_1} \\ \Delta\alpha_{r_2} \end{bmatrix} \tag{3.18}$$

The sending and receiving end controllers shown in Figures 3.4 and 3.5 are practically identical, aside from differences in lead-lag compensator parameters and the absolute values of the firing-angles. Their main difference is the independence of current on the dc voltage controller at the receiving end.

The back to back link is bi-directional and when a power flow direction change is specified, the following process is initiated. The active power is decreased to zero, and the dc voltage order is raised to maximum to speed up active power reduction (by actively reducing dc current). Upon the measured dc power and dc current reaching zero, the dc voltage order is set to zero, and once that is reached, both the sending and receiving end thyristor firing circuits are blocked. Then the integrators on each of the control channels are reset to their initial positions of $\pm 90°$ for the new sending and receiving ends. Active power control is then passed to the new sending end and the real power and dc voltage controls start up in the opposite direction.

With the linearisation methods used in Figures 3.4 and 3.5, reactive power control is possible regardless of ac system strength. Terminal voltage control on the other hand is more difficult with a greater effect on voltage stability, and is therefore critical in weak systems, where a drop in terminal voltage at the sending end reduces the maximum available power transfer. To achieve stable terminal voltage control, a more suitable configuration for each end of the link is illustrated in Figure 3.6.

This diagram shows that the RMS terminal voltage is calculated from each of the phase voltages (V_{T_a}, V_{T_b}, V_{T_c}), and is then compared to a nominal terminal voltage set-point $V_{T_{(ref)}}$. The error signal developed is fed through an enabling multiplier which prevents terminal voltage control in the absence of real power transfer. The enabler is rate limited to provide a damped ramp up of the error signal. The PI controller outputs a reactive power order ($Q_{T_{(ref)}}$) which is hard limited to prevent saturation of the controller output.

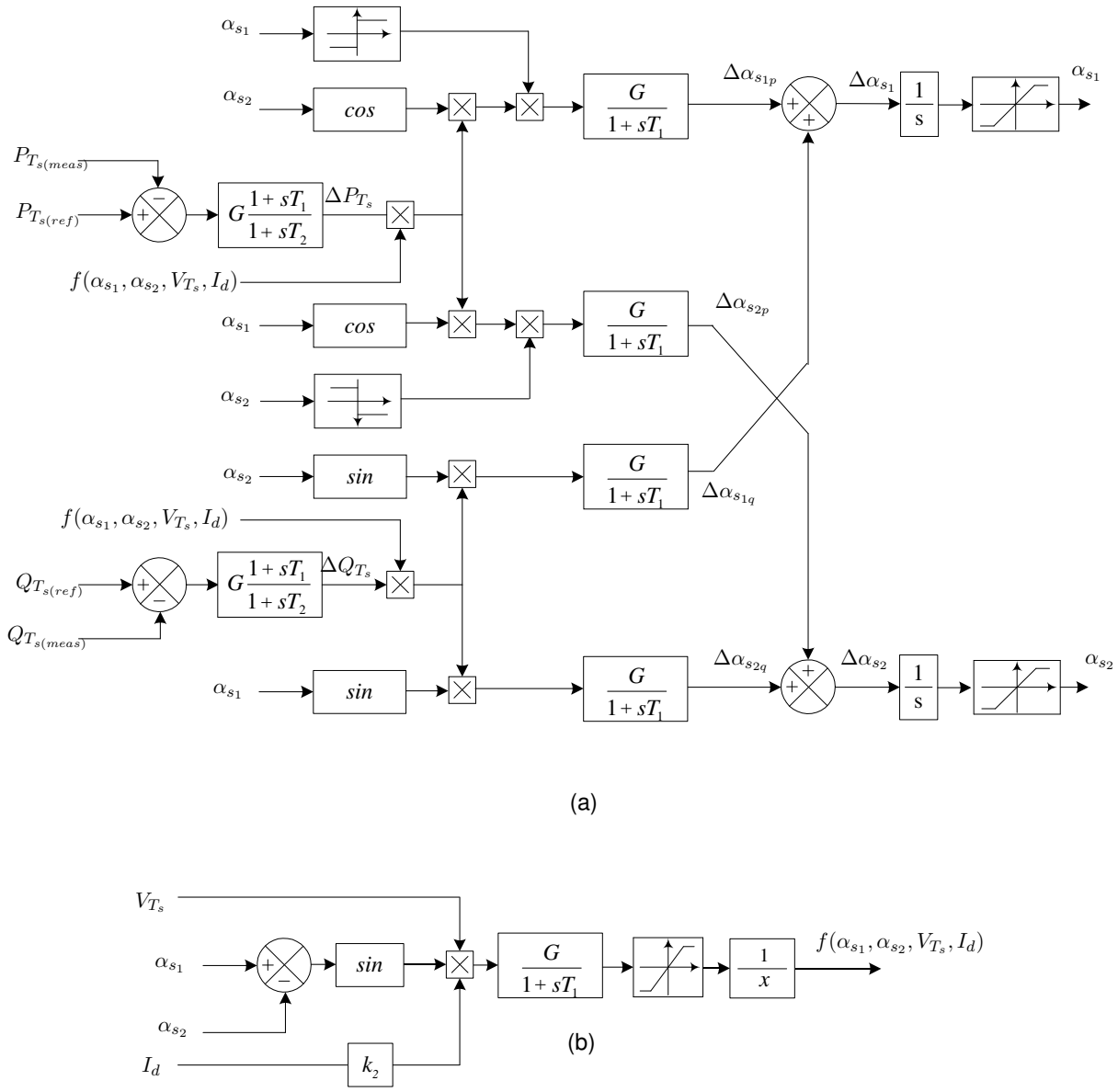


Figure 3.4 Sending end MLCR real and reactive power controller

3.5 DYNAMIC SIMULATION

3.5.1 Test System

The test system in Figure 3.7 is based on a series-parallel MLCR back to back link, with both ends supplied by Thevenin sources representing supply networks with SCRs of approximately 2. Each Thevenin source supplies 500 kV through a series reactance of 0.3617 H to a common terminal bus, where two paralleled three-winding 700 MVA transformers provide 50 kV to each of the 48-pulse MLCR converters. The rectifier and inverter are connected via a dc bus, with a 1.5 H smoothing reactor and a total resistance of 100 mΩ.

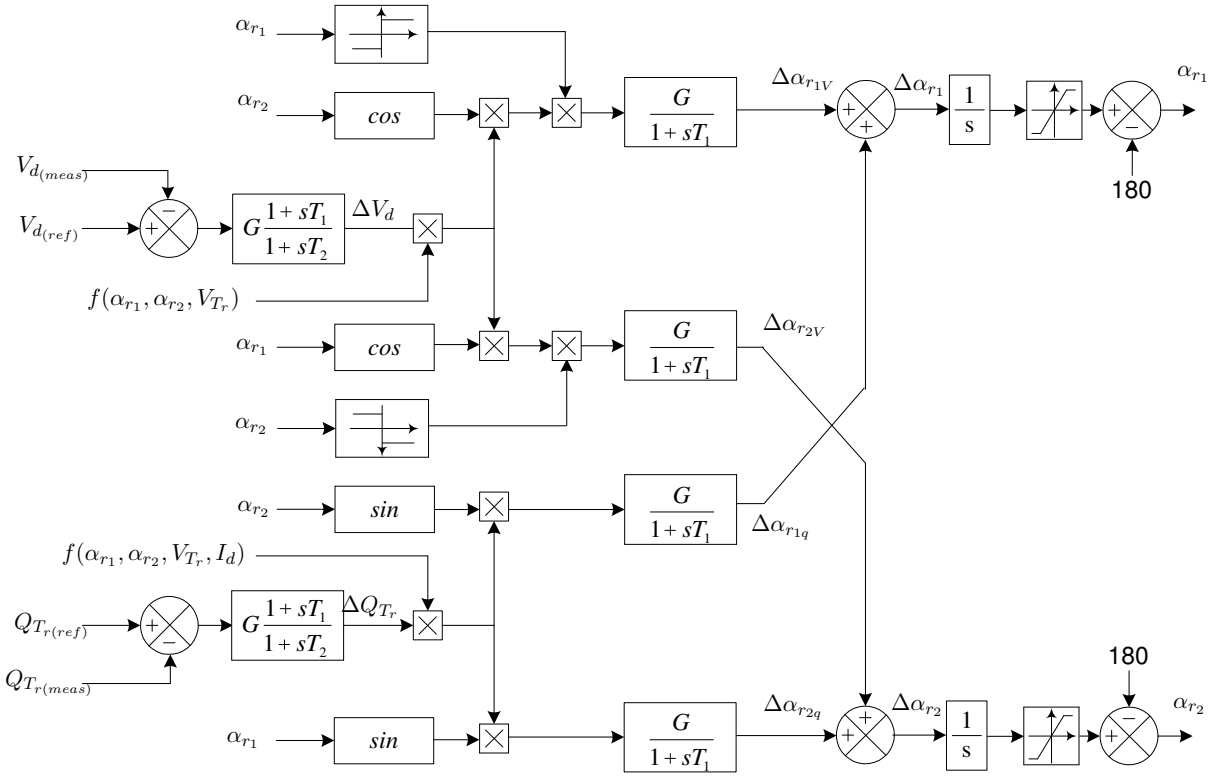


Figure 3.5 Receiving end MLCR real and reactive power controller

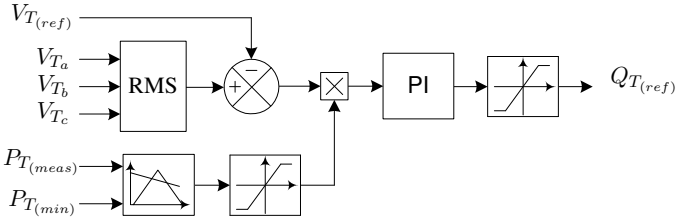


Figure 3.6 Terminal voltage control used at both ends of the link

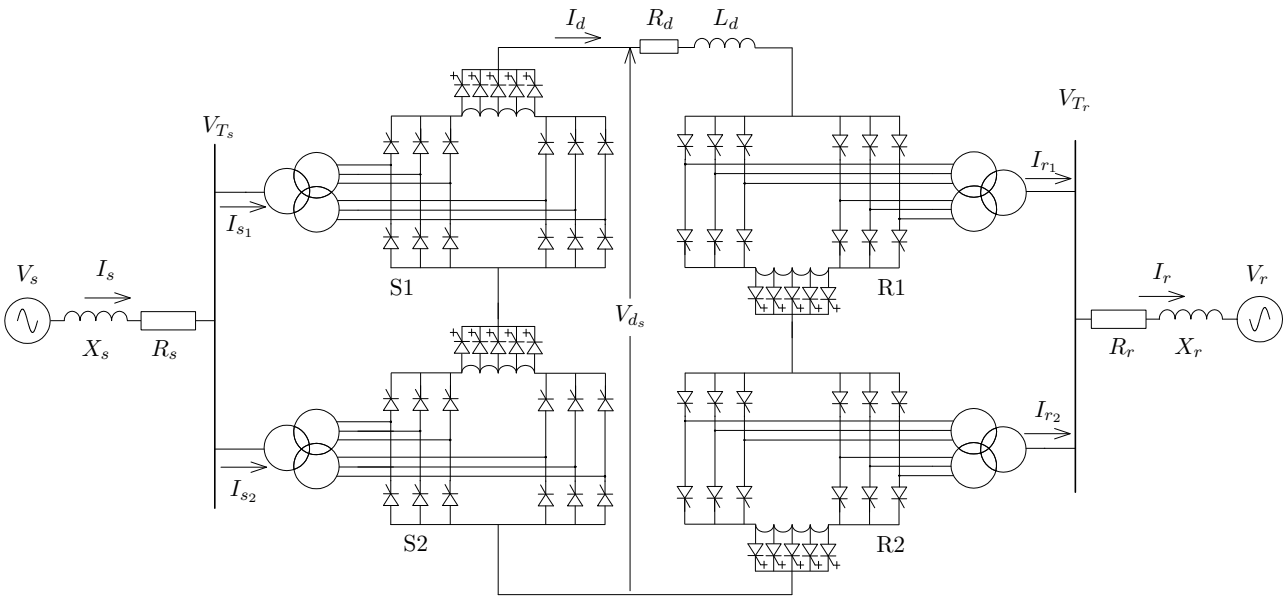


Figure 3.7 Back to Back series-parallel MLCR test system

3.5.2 Simulation Verification

The test system is simulated using PSCAD/EMTDC over an 8-second period. The objective of the simulation is to verify the bi-directional transmission capability of 1100 MW, whilst controlling terminal voltage, and varying the dc voltage between minimum and maximum of 50 kV and 120 kV respectively. The simulated results are shown in Figure 3.8.

The link operation starts at t=0.1 s. Graph 3.8(a) shows the sending end real power order (1100 MW), the measured power and the reactive power generation (Q_{T_s}) at the common ac terminal controlled to maintain V_{T_s} constant at 500 kV (1pu). The reactive power controllers are automatically enabled when active power increases over 5MW, thus preventing attempted operation with negligible dc current. The receiving end terminal's active power is shown in graph (f), the difference between the sending and receiving end terminal powers is approximately 9% (from $t = 0 - 1.5s$), which is made up of dc, switching and transformer losses. The losses increase to almost 40% at minimum rated dc voltage, due to the doubling of dc current (losses $\propto I_d^2$) and corresponding larger ac current circulated between the leading and lagging converters at both ends.

The dc voltage order, shown in bold trace in graph (d), is 120 kV from $t = 0$ to 1.5s together with the corresponding measured dc voltage. α_{1_s} and α_{1_s}, the sending end firing-angles (graph (b)) reduce to 1.6° and −37.9° respectively, with one converter at maximum dc voltage and the other supplying the reactive power compensation; this provides the most efficient sending end operating point. At $t = 1.5s$ the dc voltage is reduced to 50 kV, which is achieved by decreasing α_{1_r} and increasing α_{2_r} at the receiving end (graph(g)), the actual values sent to the thyristor

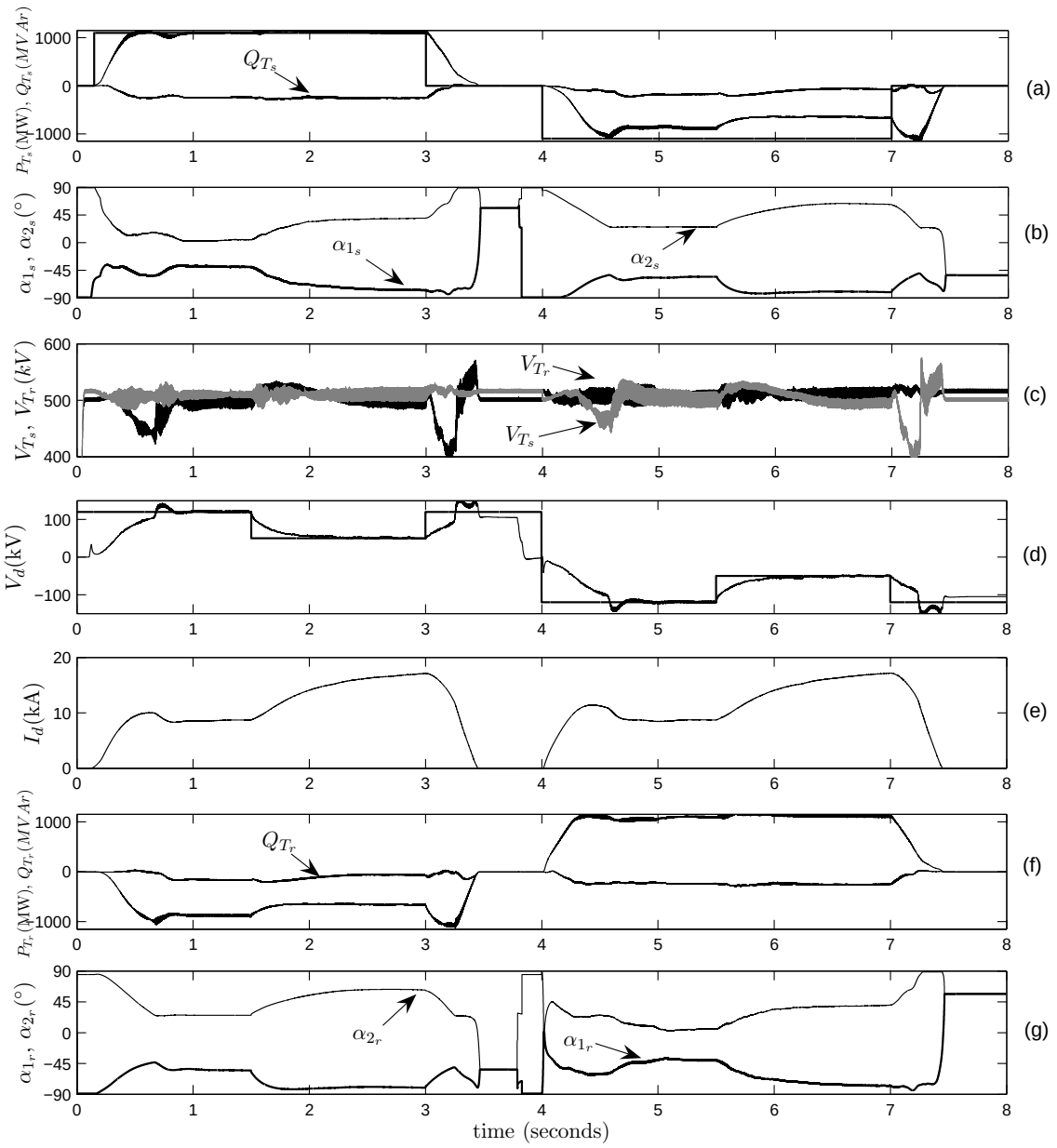


Figure 3.8 1100 MW MLCR Back to back link simulation over an 8-second period, with (a) real and reactive power contributions of the sending end in, (b) firing-angles , (c) terminal voltages, (d) dc voltage, (e) dc current, (f) receiving end real and reactive power in, and (g) firing-angles

firing logic being $(180° - \alpha_{1_r})$ and $(180° - \alpha_{2_r})$, valid from 0 to 3.4 s. The change in firing-angle results in an increased dc current (graph (e)) and a shift in the two sending end firing-angles, as seen in graph (b) from 1.5 to 3.0 s. The effect on the sending end active power is negligible, and only a small change in terminal voltage observed (Figure 3.8(c)), which is quickly corrected by an increase in $Q_{T_{order}}$. A drop off in V_{T_r} of approximately 10% is observed between 0.4 and 0.8 seconds as the receiving end reactive power control is established; the control of Q_{T_r} is intentionally made slower than the dc voltage control so that stable dc current is maintained;

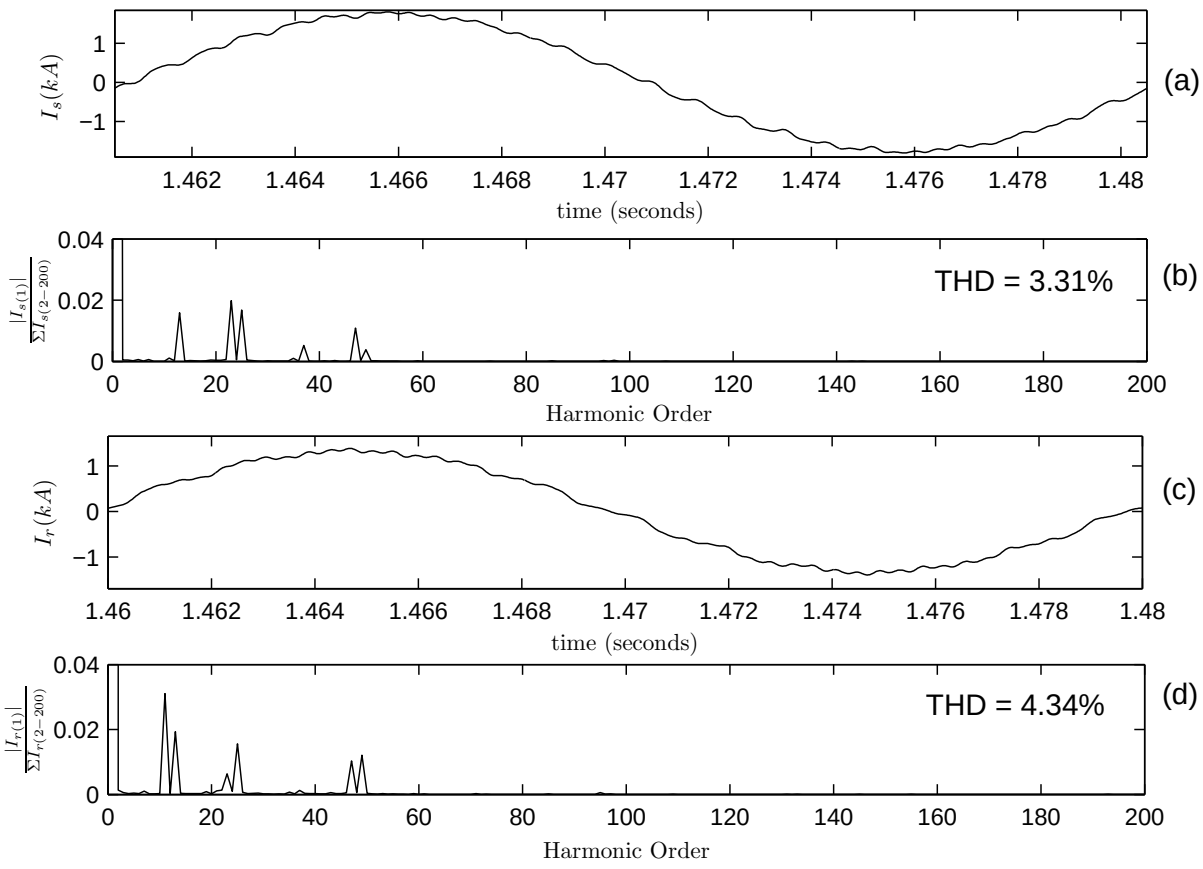


Figure 3.9 Harmonic performance of the sending (rectifying) and receiving (inverting) end supply waveforms for the first 200 harmonic orders

otherwise interaction between the sending and receiving reactive power controllers would occur.

At $t = 3.0s$ a reversal in active power flow direction is ordered. The active power is ramped down, and the dc voltage control order raised to reduce dc current. When the dc current falls to zero at $t = 3.5s$, $V_{d_{order}}$ is decreased; at $3.85s$ the main thyristor bridge firing circuits are disabled, and the duties of the active power and dc voltage controllers exchanged between the two ends. The dc current is not maintained during the direction reversal, in part due to the reactive power control required during the direction change, and because of the limitations with the PLL blocks in the PSCAD/EMTDC simulation environment. If during a real power direction reversal (where $\pm 180°$ PLLs are used) a firing-angle change from $-179°$ to $179°$ can either pass through $180°$ or $0°$, the consequences can be potentially catastrophic. When 4 firing-angles must be coordinated simultaneously, the process becomes even more impractical.

At $t = 3.85s$ the firing-angle origins are reset to $\pm 90°$ and the controllers re-enabled, the same 1100 MW order applied to the new active power controller at $t = 4.0s$. The dc voltage is then varied as with the first half of the simulation.

Thus the simulated test results validate that the back to back MLCR link provides independent reactive power control between two weak power systems.

3.6 WAVEFORM QUALITY

The current waveforms and harmonic components of the sending and receiving ends are shown in Figure 3.9. The characteristic harmonic magnitudes for the sending end (rectifying) are 1.5% for the 13^{th}, 1.9% 23^{rd}, 1.8% $25^{th}$and 1.3% for the 47^{th}, with a total harmonic distortion (THD) of 3.31%. At the receiving end (inverting), the characteristic harmonics are 3.1% for the 11^{th}, 1.9% 13^{rd}, 1.5% 25^{th}, 1.0% 47^{th} and 1.1% for the 49^{th}, with a THD of 4.34%.

3.7 CONCLUSIONS

The independent controllability of reactive power between the ends of an MLCR back to back link has been clearly established, and its suitability for bi-directional large power transfer between two weak systems demonstrated. The ability to control dc voltage and current directly, whilst still satisfying reactive power demands at both ends has been validated. Satisfactory harmonic performance of the hybrid series-parallel configuration has also been proven, without the need for harmonic filtering, with THDs of 3.31% and 4.34% measured under rectification and inversion respectively.

All of these attributes make the back to back series-parallel MLCR ideally suited to high power transfer with the same flexibility of PWM control, but with the efficiency and rating of conventional thyristor based converters.

Chapter 4

FAULT RESPONSE OF MLCR UHVDC TRANSMISSION

4.1 INTRODUCTION

The use of Ultra High Voltage DC transmission (UHVDC) will be required in the near future to economically transmit energy from the largest hydro-electric schemes to rapidly expanding load centres [33]. UHVDC links will be expected to transmit more than 2000 MW, with distances in excess of 1000 km. At these power levels, thyristor based HVDC conversion is the only economic option, with series connected converters configured for high pulse operation and to achieve the required dc voltage rating. With such large power extracted from remote regions, minimising the ac current through high power-factor operation is essential for efficient operation.

The multi-group HVDC current source conversion transient performance was proven in Chapters 2 and 3, with firing-shift control enabling an extra degree of control freedom to further increase HVDC transmission efficiency. By controlling power-factor at the ac terminal, the ac current may be minimised, independent of the dc voltage which is maintained at rated dc voltage for all active power levels. In this way both the ac and dc losses may be minimised for all operating conditions.

The multi-level topology, with line commutated thyristors in the main converter bridges, provides the flexibility of self commutated switching schemes, but with improved efficiency and lower cost for a given rating. The switching characteristics of the multi-level current reinjection (MLCR) current sourced converter (described in Appendices A and B), although similar to conventional high pulse line commutated conversion, are achieved without a commutation period and without the restriction of an extinction angle. This behaviour for either leading or lagging operation must thus be tested for both normal and abnormal operating conditions, the latter including single phase and three phase ac faults at both converter ends, and dc short-circuit recovery.

This chapter summarises the analysis of the multi-group MLCR UHVDC converter under ac and dc fault conditions.

4.2 TEST METHOD

The multi-group firing-shift HVDC converter is subjected to both ac and dc faults in accordance with the Cigre acceptance testing criteria as given in [34]. The ac fault magnitude and duration is calculated such that converter terminal voltage drops to 0.7 per unit and is maintained for 0.1 s. The ac faults are initiated at each of the sending and receiving ends to simulate disturbances in the power system. Each fault is located at the mid point of the system impedance when considered as a Thevenin equivalent, an example for an arbitrary system is given in Figure 4.1 with the terminal voltage represented by V_T. Similarly on the dc side the fault is located at the midpoint of the dc link.

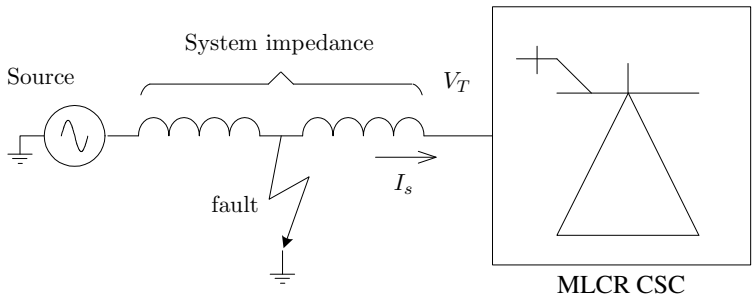


Figure 4.1 Location of the ac faults at the mid point of the system impedance

The expected converter operation during the fault is either to ride through with minimum disturbance, to reduce rated power output during the fault, or to power down and resume normal operation when the fault clears. In the event of a dc fault, the current source converter is expected to control current to zero to extinguish the fault arc, and then attempt to resume normal operation.

The power systems at each end of the link are represented by Thevenin equivalents, with short circuit ratios (SCRs) of 3. These are used to make converter terminals appear weak, and make the resulting fault conditions realistic.

4.3 TEST SYSTEM

The test system in Figure 4.2 consists of a uni-directional bi-pole UHVDC interconnection, capable of 2000 MW real power transfer on an ±800 kV dc link. At each end of the link, two 48-pulse MLCR converter blocks with ratings of 1000 MW each are series connected, and the centre point of the sending end series connection is grounded as a reference for the insulation coordination of the scheme. The source voltages are set at 1.06 and 1.0 pu at the sending and receiving ends respectively.

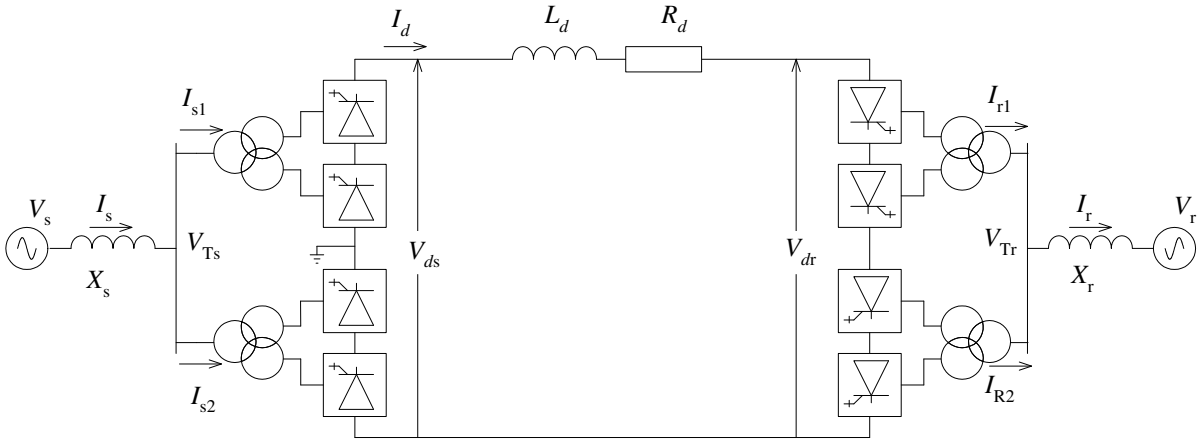


Figure 4.2 2000 MW ±800 kV UHVDC Test System

4.3.1 Control system

To ensure full active and reactive power control of the MLCR UHVDC converter's strong non-linear system, a similar linearisation technique to that of Chapter 2 is employed, but with cascaded active power, dc current and dc voltage loops to maximise dc voltage (and thus minimise dc current) for a specified active power. The cascaded configuration also ensures correct operation during faults, and acts to restrict the converter to its voltage and current ratings during disturbances.

Cascade control loops

Figure 4.3 shows the control block diagram for the sending end with, from left to right, top to bottom, the active power, dc current, dc voltage and reactive power control loops.

The outer most loop generates an error signal from the difference between active power order ($P_{Ts_{ref}}$) and measured sending end power (P_{Ts_m}). The error is fed into a lead-lag compensator that derives the dc current order ($I_{ds_{ref}}$), which is in turn hard limited and compared to the measured dc current (I_{ds_m}), from which the dc current error signal is generated. A second lead-lag compensator derives the sending end dc voltage order which is constrained to rated dc voltage and passed to the inner most loop, the dc voltage controller. The dc voltage order ($V_{ds_{ref}}$) is compared to the measured dc voltage (which is low pass filtered to remove switching spikes), the resulting error signal fed into a third lead-lag compensator. The compensator output is an incremental dc voltage order (ΔV_{ds})which when combined with Figure 4.4 is used to interface with the strongly non-linear converter response, making it appear linear.

Similarly the reactive power controller interfaces with the converter in the same way and is

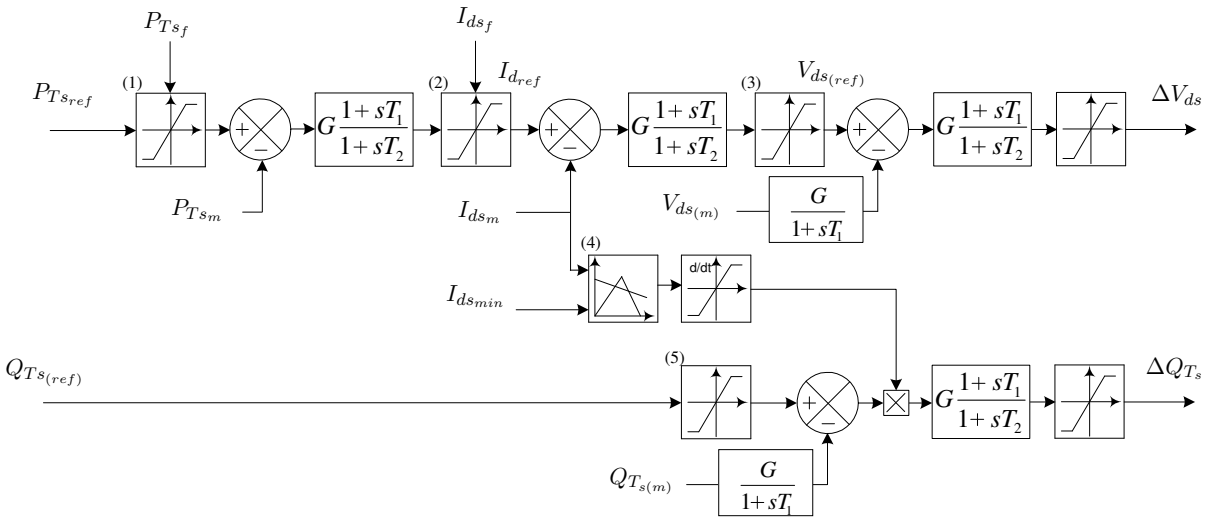


Figure 4.3 Linear component of the Sending end active and reactive power controllers

explained in the next section. Since reactive power controllability depends on dc current, the channel is enabled when the dc current exceeds a minimum threshold (by block $^{(4)}$) and a ramping function ensures a bumpless transfer from zero to the specified control order ($Q_{Ts_{ref}}$). The reactive power error signal is fed into a lead-lag compensator and the subsequent output (ΔQ_{Ts}) is used at input to the reactive power channel of the non-linear mapping function.

The hard limit blocks in each of the three control loops restrict the terminal active power to 1.0 pu, dc current order to 1.2 pu and the dc voltage order to 1.10 pu (shown as $^{(1)}$, $^{(2)}$ and $^{(3)}$ respectively in the figure). Similarly the reactive power order is restricted (by $^{(5)}$) to 100 MVAr absorption and 500 MVAr generation during normal operation. During faults where power flow must be interrupted, the hard limits clamp the active power order and dc current order to low levels, using the P_{Ts_f} and I_{ds_f} control inputs in Figure 4.3.

The controller gains for each of the lead-lag compensators are given for the active power, dc current, dc voltage and reactive power in Table 4.1.

Table 4.1 Sending end Controller parameters

Parameter	Active Power	dc Current	dc Voltage	Reactive power
k_P	0.31	0.085	40	19
k_I(s)	0.17	2.35	0.005	0.0025
k_D	0.0001	0.0	0.0001	0.0

Linearising interface to the converter firing logic

The linearising function is given in Figure 4.4, and is used at both ends of the link to make the strongly non-linear converter appear linear to the cascaded control loops of Figure 4.3. The layout is based on the control theory of Chapter 3, derived from equations (3.16) to (3.18). The integrator time constant determines the overall bandwidth of each of the control channels and is set to 2 ms for the scope of this analysis.

The layout of the incremental voltage (ΔV_{ds}) and reactive power (ΔQ_{T_s}) channels are very similar, the main exception being the control action reversal required in the voltage channel, when a firing-angle changes quadrants, as identified by $^{(1)}$ and $^{(2)}$ in Figure 4.4(a). With the dc voltage control, for very small firing-angles (with $\cos(\alpha) \approx 0$) where a change from one quadrant to another occurs, oscillation about the axis may result and so is damped by a low pass filter with a 1ms time constant.

With respect to the common components of Figure 4.4(a), the sine and cosine functions set the gain of the opposing firing-angles, in combination with the calculation of Figure 4.4(b) which determines the overall gain by the displacement between the two firing-angles, terminal voltage (V_{Ts_m}) and measured dc current (I_{ds_m}) in the case of the reactive power channel.

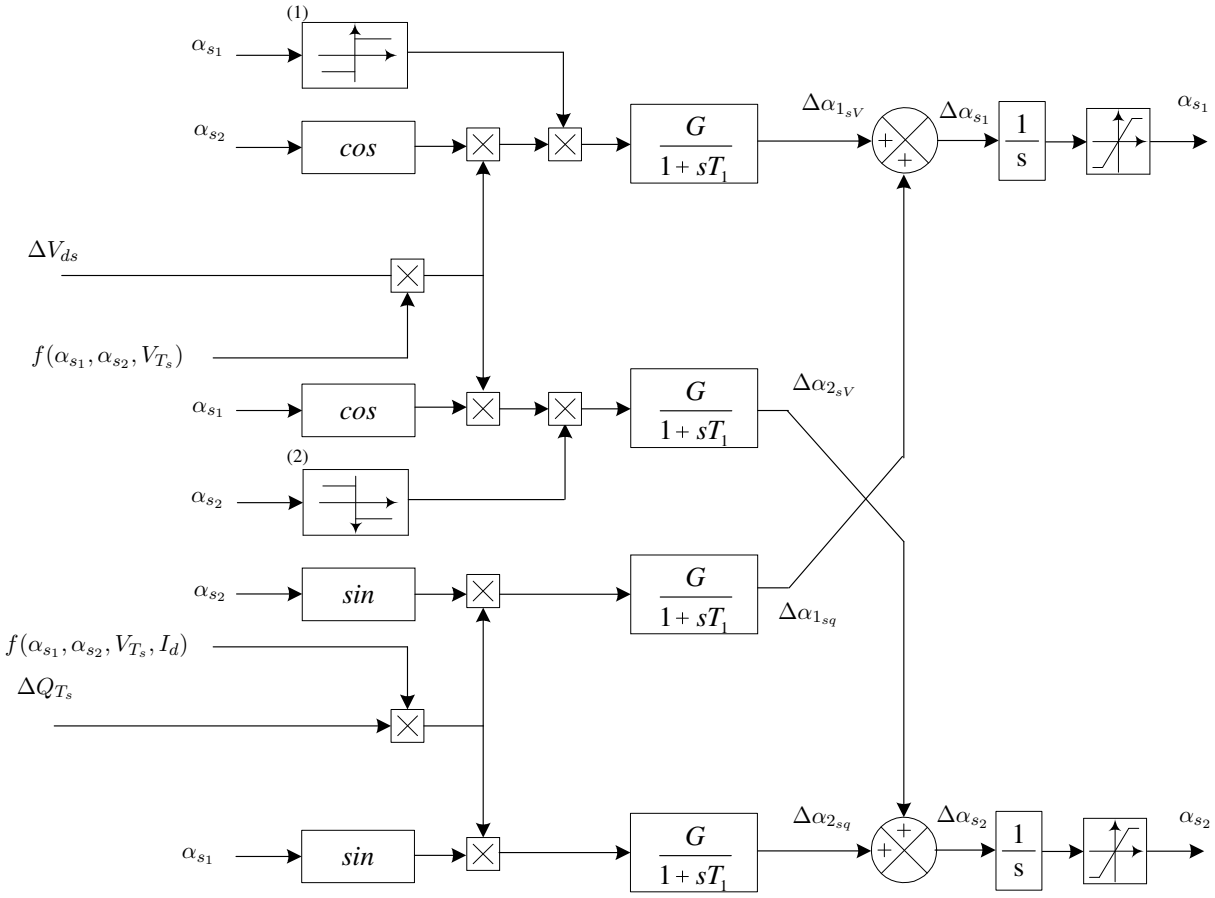
Firing-angle reference

An accurate firing-angle reference is critical to stable converter operation, particularly during large fault transients. The method, shown in Figure 4.5, is used for full range firing-angle control. A phase locked loop (PLL) is used in each current source converter, its reference derived from the instantaneous measurement of each of the terminal phase voltages. Although the supply current waveform has minimal distortion in a current source converter, the voltage distortion due to switching is pronounced, and increases the weaker a system becomes.

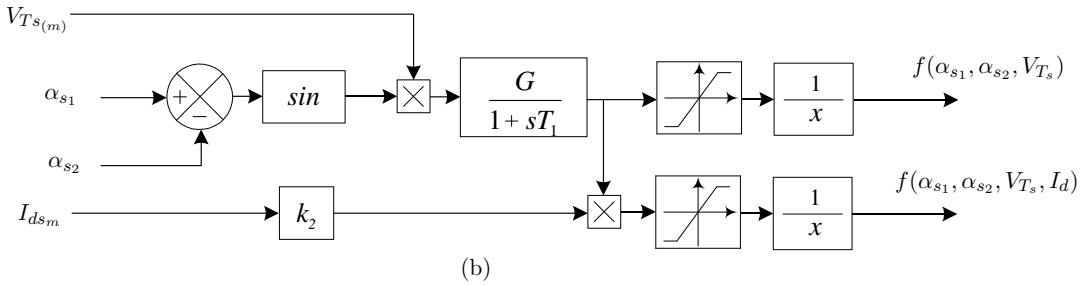
A bandpass filter is used to minimise high freq disturbances, to accurately track phase-shift during dynamic changes and provides a smooth 3-phase voltage waveform to the PLLs. The output is used to generate 12 synchronised ramping signals, one for each of the main bridge thyristors, and a further set of firing pulses at six times the fundamental frequency to the 5-level reinjection circuit to enable 48-pulse operation.

Fault logic

A simple method for determining when a fault has occurred is used in this analysis. The fault diagram in Figure 4.6 interfaces with the cascaded control loops to reduce the control order of the active power and dc current when an abnormal operating condition is detected. A reduction



(a)



(b)

Figure 4.4 The non-linear mapping functions of the Sending end voltage and reactive power controllers

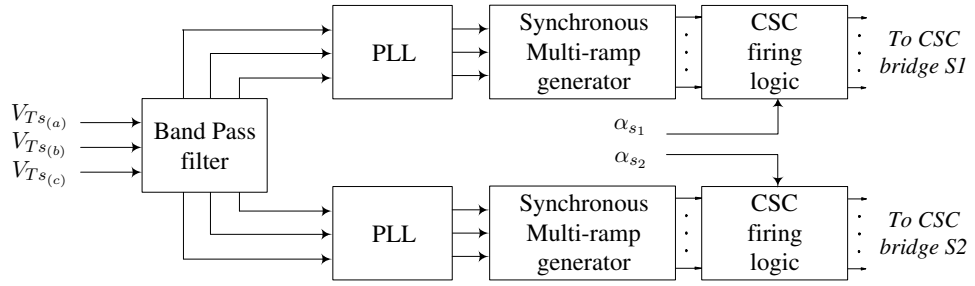


Figure 4.5 Sending end MLCR converter firing-angle reference

in control order is initiated when either the measured terminal power (P_{Ts_m}), dc current (I_{ds_m}) or dc voltage (V_{ds_m}) exceed their respective maximum ratings, which are 1.25pu, 1.2pu and 1.1pu respectively. The fault condition is reset when the three measured values fall below a minimum value, which for this analysis has been selected as 0.01pu, 0.0pu, and 0.9pu for the power, current and voltage loops respectively.

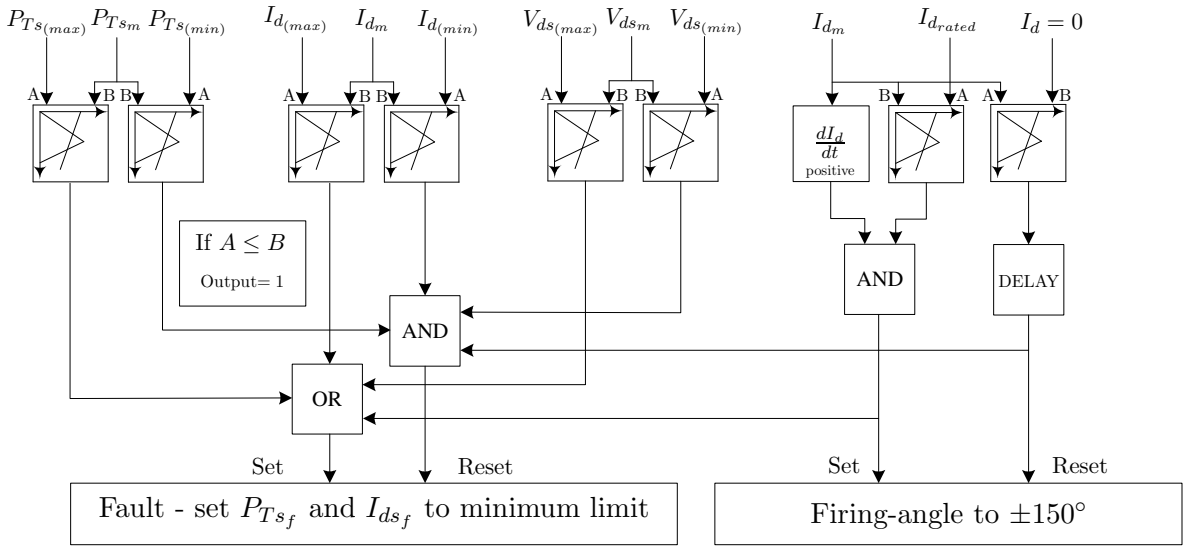


Figure 4.6 Sending end fault logic

The method of dc fault detection and recovery in this scheme is the same as that used in conventional LCC dc links. Explained briefly, and with reference to Figure 4.6; on detection of a dc fault by positive $\frac{dI_d}{dt}$ above rated dc current, the rectifier firing-angle is delayed into inverter operation (advanced for the leading firing-angle) to 150° (-150° lead) to accelerate the fault current collapse, until the fault current drops to zero and adequate time (typically $100-200$ ms) is given for fault arc extinction and deionisation. Once cleared, the converter is restarted and attempts to return to its pre-fault active power setting as quickly as possible.

4.4 DYNAMIC SIMULATION

4.4.1 Sending end AC Faults

The sending end response to single phase and three phase ac faults are plotted in Figure 4.7, with the corresponding receiving end waveforms shown as dashed traces in each of the graphs for comparison. The sending end fault is initiated by placing an impedance in shunt at the midpoint of the system impedance, of 0.03 H in series with a 1.25 Ω resistor for the single phase case and a 4 Ω resistor for the 3 phase case.

At $t = 1.5s$ a single phase fault is applied to phase A, the terminal voltage in (b) dropping to 81.77 kV, or approximately 0.64 pu, with the other sending end phases dropping to 0.93pu. In sympathy with the drop in terminal voltage, the dc current reference ($I_{d_{ref}}$) increases (in (c)) to attempt to maintain power flow, as does the dc voltage order ($V_{ds_{ref}}$) in Figure 4.7(d). The fault clears at $t = 1.6s$, at which time the converter resumes the pre-fault power flow control order, with full recovery at $t = 2.1s$. The same response is true for the three phase fault which occurs at $t = 3.0s$. The terminal voltage (b) drops to 94 kV, or 0.7 pu and recovery begins when the fault clears 100ms later. In both the single and three phase cases, the sending end firing-angles drop to zero. This causes a small overshoot in both the dc voltage and current during recovery.

The sending end ac current waveforms during the ac faults are given in Figure 4.8. In 4.8(a), the single-phase fault, phase A current drops to zero at $t = 1.51s$, while phases B and C continue with some dc bias, until the fault clears at $t = 1.6s$. The response of the receiving end phases A and B are given by the dotted lines in the graph.

The ac 3-phase fault in Figure 4.8(b) on the other hand interrupts all current flow from 3.05s with some distortion to the ac current waveform and resumes at $t = 3.11s$. Some oscillation is evident during the recovery in the receiving end current trace.

4.4.2 Receiving end AC Faults

Receiving end performance under single and three phase ac faults is given in Figure 4.9. The single phase fault is initiated at $t = 4.5s$ where a series connected 2Ω resistor and 0.02 H inductor grounds the midpoint of the system impedance. An immediate overcurrent results, as given in Figure 4.9(c), reaching 1.5 kA (1.3 pu) 35 ms after the fault is initiated, and subsequently drops to zero after a further 25 ms. Power flow resumes at 4.56 s, as given in Figure 4.9(a) with a power order of 2000 MW (1pu) and dc current rise to 1.23 kA which peaks at 4.72 s before resuming pre-fault levels at $t = 5.5$s.

A less severe three-phase fault at $t = 6.0$ s decreases the receiving end ac terminal voltage

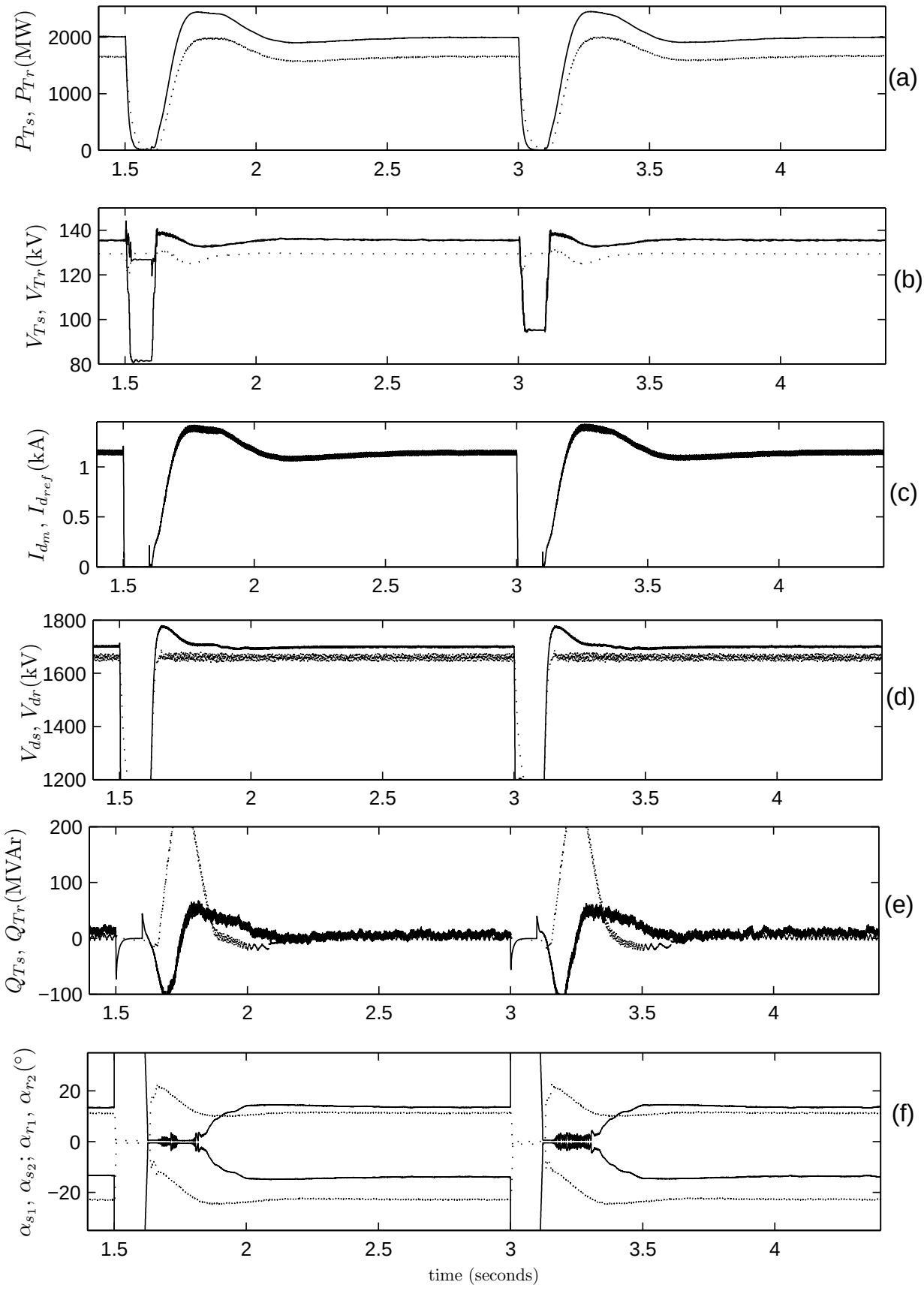


Figure 4.7 Sending end response to single and three phase faults (receiving end as · · ·)

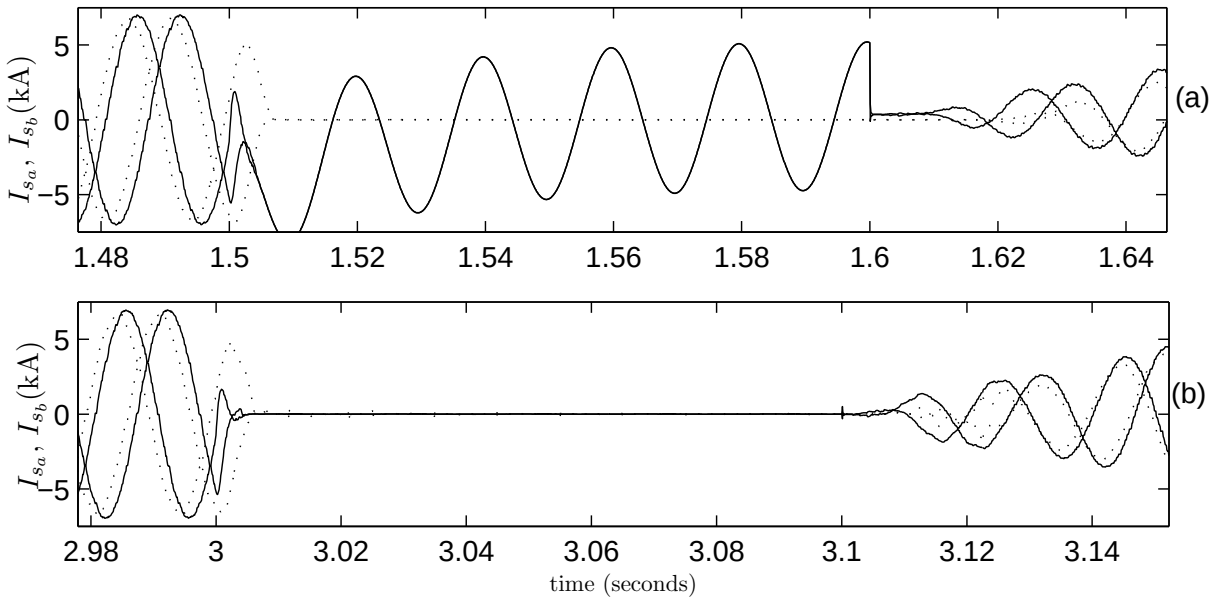


Figure 4.8 Sending end ac current waveforms for (a) the single phase fault and (b) the 3-phase fault (receiving end as $\cdots$)

(Figure 4.9(b)) to 0.85 pu, the link capable of running through with minimal disturbance aside from a small perturbation on the dc current waveform. At $t = 6.5s$ a larger 3-phase fault occurs at the receiving end consisting of a series connected 2Ω resistor and 0.02 H inductor short-circuited to ground over a 100 ms period. The receiving end terminal voltage (Figure 4.9(b)) drops to 94.5 kV, before increasing slightly to 109 kV as the receiving end converter ac current drops. The dc voltage (Figure 4.9(d)) decreases to a minimum 920 kV 50 ms after the fault is initiated, before recovering 50ms later. Once the fault is removed the controller resumes normal operation and the active power, shown in Figure 4.9(a), rises to a maximum of 2300 MW (1.15 pu) before settling 200 ms later.

The receiving end ac current waveforms are given in Figure 4.10. The single phase fault in graph (a) heavily distorts the ac current during the single phase fault, with phase A shifting to be in phase with phase B for the duration of the fault and distortion of the transformer flux causing third harmonic during recovery. The 3-phase fault also shows some residual oscillation during the recovery process (in (b)) which dies out within two cycles (40 ms).

4.4.3 DC faults

The main consideration with power transfer at such high voltages is maintaining the correct control response during faults. AC fault response is a function of the sending end voltage and system impedance and doesn't differ much as the active power rating and dc voltage rating

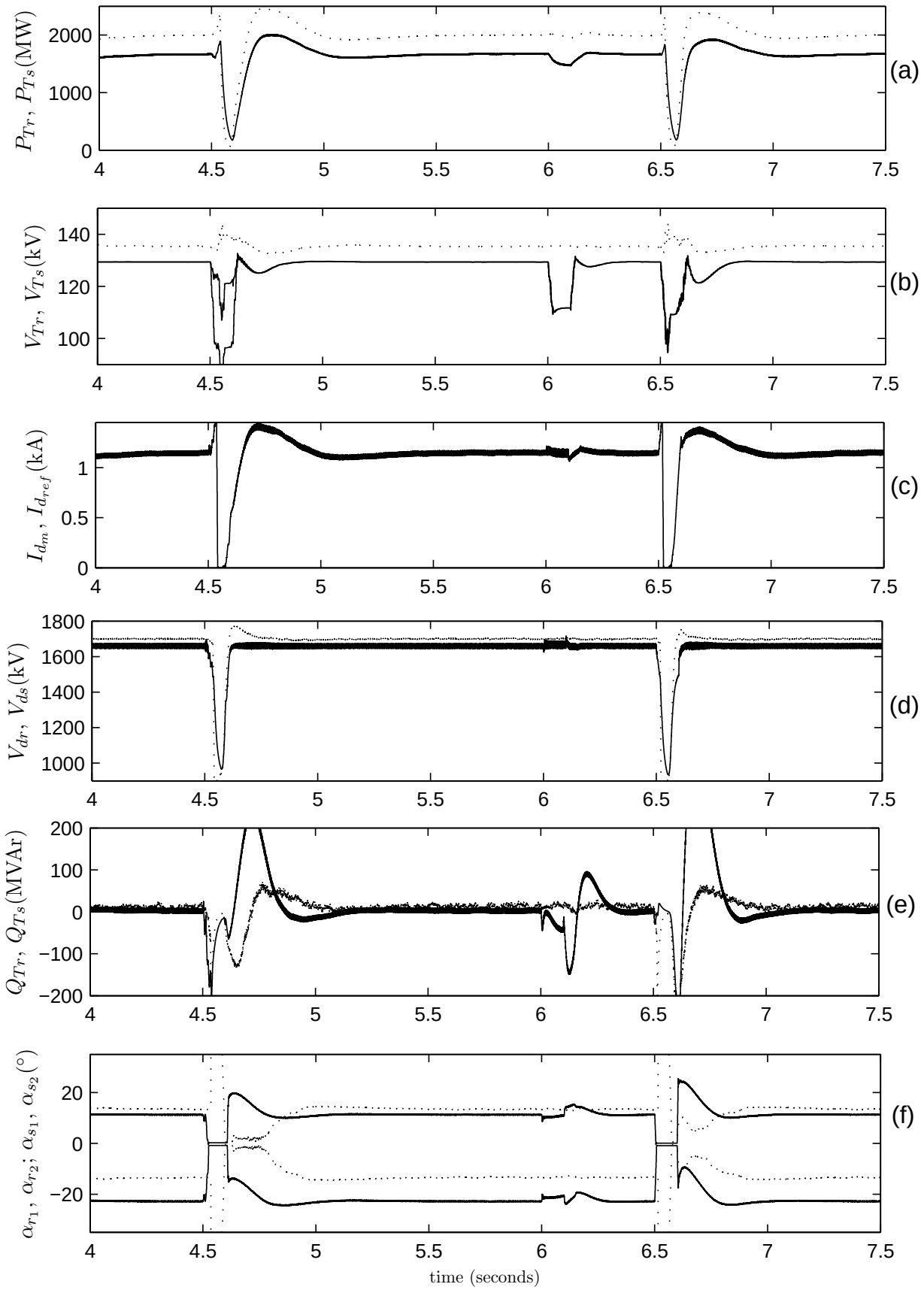


Figure 4.9 Receiving end response to single and three phase faults (the sending end traces shown as $\cdots$)

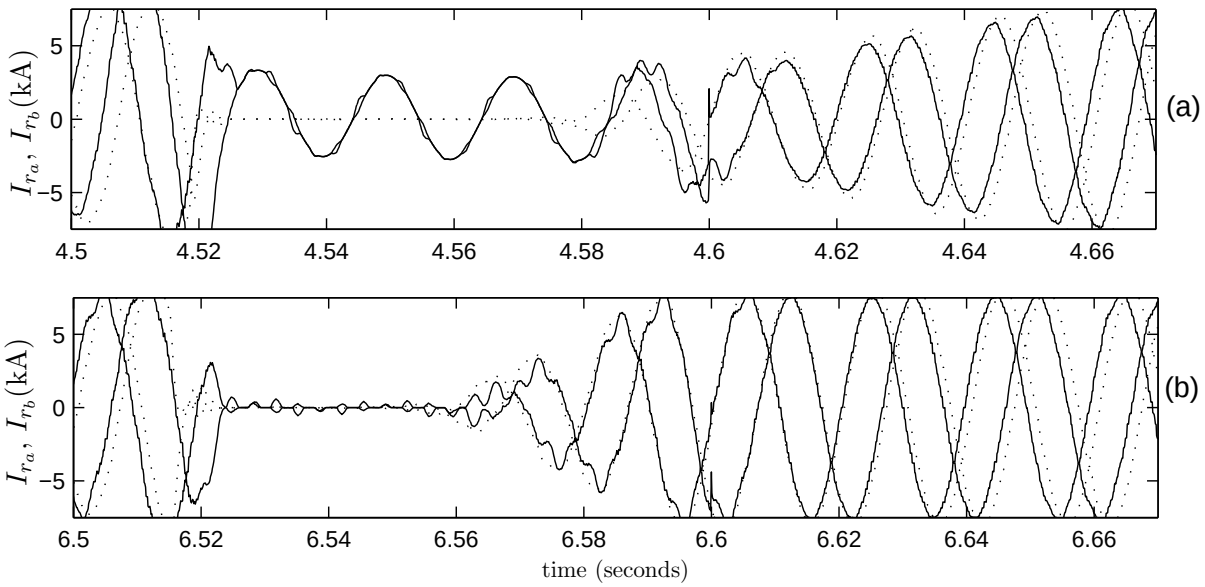


Figure 4.10 Receiving end ac current waveforms for (a) the single phase fault and (b) the 3-phase fault (the sending end ac currents shown as dotted traces)

increase. DC faults however, are (excluding control response) dependent on the dc voltage rating, total dc link inductance, and the rate of current rise during a fault.

Consider the following equation which gives the rate of current rise during a dc fault.

$$\text{Rate of fault current rise (kA)} = \frac{V_{ds_m}}{L_{d_f}} \mid_{@t=0} = \frac{dI_d}{dt} \tag{4.1}$$

The dc voltage (V_{ds_m}) is that at the sending end terminal at the instant of the fault ($t_f = 0$) and L_{d_f} is the total inductance of the fault loop (the subscript $_f$ indicating the conditions that apply during fault); for example if the fault occurs at the mid point of the dc transmission line then

$$L_{d_f} = \frac{L_d}{2} + L_{\text{fault}} + L_{\text{send end reactor}}$$

For a dc voltage of ±800kV (1600kV line to line) and fault loop (L_{d_f}) of 4H

$$\begin{aligned} \frac{1600\text{kV}}{4\text{H}} &= \frac{dI_d}{dt} = 400\text{kA}/s \\ &= 0.4\text{kA}/ms \\ &= 0.4\text{A}/\mu s \end{aligned}$$

Rated dc current in the 2000 MW ±800 kV dc link is 1.15 kA and thus the dc controller response during the fault must be able to clear rated current in approximately 3 ms or less ($\frac{1.15}{0.4} = 2.875s$), or in other words, controller bandwidth must be a minimum of 350 Hz. A bandwidth of 350 Hz would make the control sensitive to noise and potentially affect steady state performance with switching voltage ripples from the reinjection scheme (300 Hz) included in the feedback path of the voltage loop. To mitigate the need for high bandwidth control response, HVDC protection has traditionally added dc smoothing reactors to reduce the rate of dc fault current rise and direct firing-angle control when faults are detected.

The latter operates in parallel with the cascaded controllers and provides overruling protection scheme which takes over from the normal control system on detection of a fault, with the sole objective of reducing the fault current as quickly as possible, to mitigate the damaging effects.

Unlike conventional LCC conversion, where a large reactive power component is absorbed by the converter (and a corresponding decrease in terminal voltage observed) during the fault, the MLCR based HVDC scheme retains its high power-factor capability, and thus minimises its impact on the connected power system. Similarly, the speed of recovery usually limited by inverter commutation failures in weak systems [35] does not feature here.

In Figure 4.12, the dc fault is initiated at $t = 1.3s$, where a 1Ω load short-circuits the mid point of both dc transmission lines together. The fault logic of Figure 4.6 correctly detects and overcurrent, with the rate of dc current rise above the maximum permitted at rated power flow , as seen in Figure 4.12(c). Within 2ms of the fault occurring the current rises to 1.45 kA before dropping to zero in under one cycle (20 ms), the total sending end power ((Figure 4.12(a)) and dc voltage ((Figure 4.12(d)) dropping to zero in under 2 cycles (40 ms), with minimal overshoot.

The terminal voltage of the sending end ((Figure 4.12(b)) rises during the fault to 143 kV (1.13pu) before dropping back to 133kV (1.05pu) some 40 ms later. The terminal voltage at the receiving end drops by a similar magnitude and returns to the pre-fault level.

The sending end firing-angles of Figure 4.11(f) maintain ±150°, while the receiving end moves to (and is limited at) ±180°. At the same instant of fault detection the active power order ($P_{T_{ref}}$) is reduced to zero. Once the fault is cleared and 200ms allowed for fault arc deionisation, the link is restarted. There is some brief oscillation of reactive power at the receiving end during recovery as seen in Figure 4.9(e) but that quickly dies away.

The dc fault interrupts both ac currents, their traces given in Figure 4.12(a) and (b) for the sending and receiving ends respectively. The strong control action required to arrest the dc current rise causes a sharp drop in the sending end ac current and some residual ringing for almost 10ms. Both end waveforms resume undistorted approximately 240ms later.

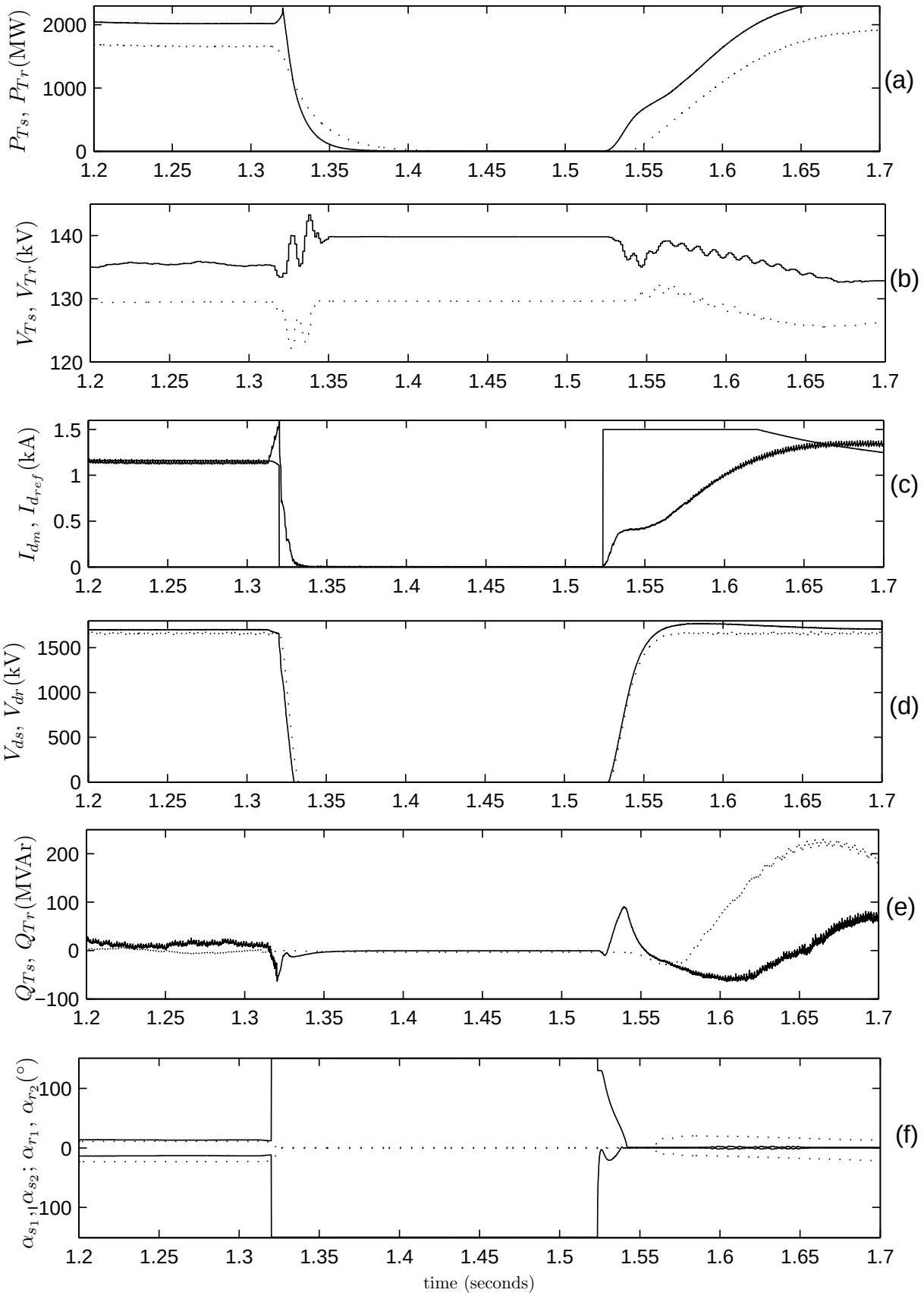


Figure 4.11 MLCR HVDC link response to a dc fault (receiving end shown as dashed trace)

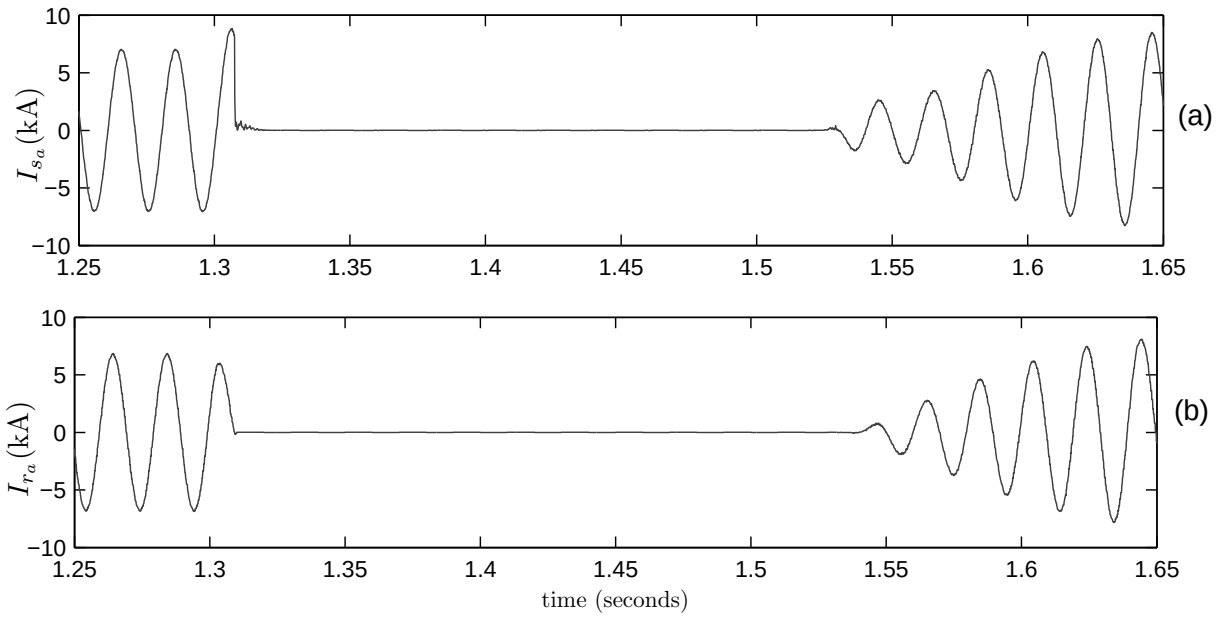


Figure 4.12 Sending end ac current during dc fault in (a) and receiving end in (b)

4.5 CONCLUSIONS

The UHVDC multi-group MLCR based high power-factor transmission system has been proven to efficiently recover from both ac and dc faults with minimal effect on the connected ac systems. With an average recovery of under 0.5 s in all ac faults and almost identical performance, coupled with just 0.7 seconds for detection, clearing and recovery of hard dc faults, this flexible current sourced topology provides predictable and repeatable performance under large system disturbances.

Chapter 5

TWO-QUADRANT POWER CONTROL FOR LARGE-CURRENT LOW-VOLTAGE RECTIFICATION WITH REFERENCE TO ALUMINIUM SMELTERS

5.1 INTRODUCTION

The control of reactive power in present aluminium smelters requires a combination of passive compensation (in the form of filters and shunt capacitors) and expensive (both in equipment cost and maintenance) transformer On Load Tap Changers. Although the current ratings of thyristor switches with turn-off capability, such as the IGCT, have already reached levels that make them suitable for use in large current self-commutating rectification, the latter is unable to control the reactive power independently from the demand of active power. The reason is that the active and reactive powers in the rectification process vary in opposite directions, because adjusting the dc current is achieved by varying the dc voltage, which is itself determined by the cosine of the firing-angle (α), while the reactive power depends on the sine of α.

With power ratings in hundreds of MW, the very large currents involved require the parallel connection of rectifier groups, each group consisting of a number of parallel-connected six-pulse bridges, with their interface transformers phase-shifted with respect to each other to produce high-pulse numbers to eliminate the need of low-order harmonic filters.

As the dc voltage does not depend on the sign of α, the multi-bridge configuration provides the opportunity of controlling the reactive power by firing one of the groups with positive and the other with negative firing-angles (in fact, the lagging current group could even be based on conventional thyristors). Accordingly, the rectifier configuration proposed in this chapter is a combination of line-commutated and self-commutated current source converter groups. The use of phase-shifting transformers is maintained, but passive compensation and OLTC are eliminated.

A review of existing smelting technology is first given. Then several alternative current source configurations are discussed, with applicability of both line commutated and self commutated

switches considered. For each multi-group scheme the theory of operation is verified by means of EMTDC simulation.

5.1.1 Review of existing smelter technology

Conventional high-current smelters supply low voltage, high dc current to one or more potlines, consisting of many series connected cells, with an applied dc voltage of 1 kV to 2 kV, and current at hundreds of kA.

The applied dc voltage is controlled using a combination of on-load tap-changers (OLTCs) for large steps in voltage and saturable reactors for fine control. With dc current in excess of several hundred kA, several OLTC/saturable-reactor dc supplies are parallel connected, a typical example given in Figure 5.1.

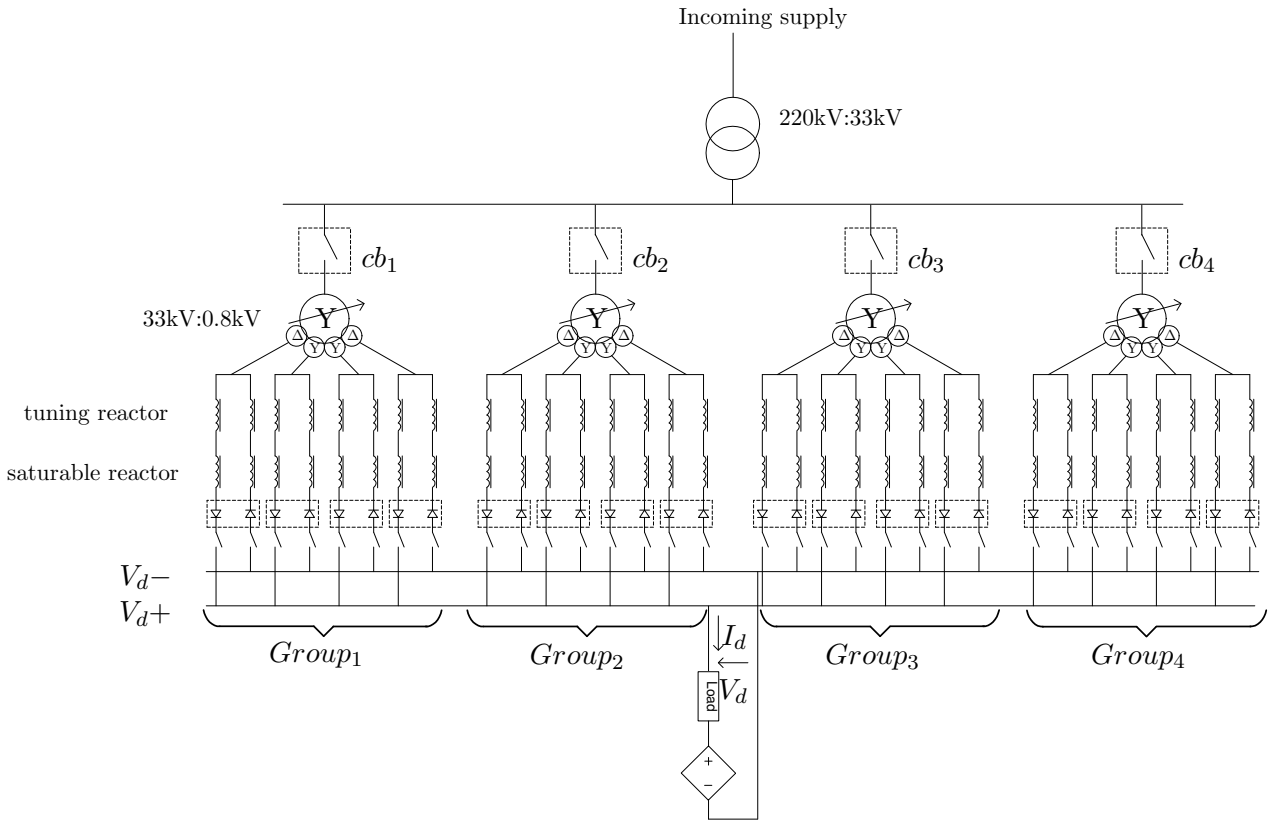


Figure 5.1 Typical smelter power system configuration

Here, four zig-zag wound phase-shifted transformers with multiple secondaries are parallel connected on both the ac and dc sides, providing a common dc bus voltage to the load. Fine dc voltage and therefore current adjustment is made by controlling the dc excitation current of the saturable reactors, with an on-load tap-change made when reactor voltage is out of range. This electro-mechanical process has several deficiencies, the first being that tap position change is

relatively slow and being a mechanical device, must be taken out of service for regular maintenance.

Secondly, tap changes and saturable reactor adjustment are made continuously during normal operation, and given the small differences in manufacturing tolerance between each rectifier, differences in reactor bias current and even tap position can occur. Realisation of ideal phase-shift, and thus harmonic performance, rely on equal transformer leakage reactances and balanced dc current, a situation not possible with this method of control.

Also, minimum tap-change position of each zig-zag transformer is limited to around 10%, and thus to fully remove power, the circuit breakers, (cb_1 to cb_4 in Figure 5.1) must be opened. Likewise, establishing power supply, either from cold or resuming from a power interruption, must begin at 10% full dc voltage, with a corresponding and undesirable disturbance to the ac terminal voltage when the breakers close. Smelters with weak transmission systems are more susceptible to terminal voltage variation with changes in operating conditions, a case common when smelters are constructed in coastal locations far from generation, for access to deep sea ports for export. Voltage support is installed, as in the examples in [36, 37] with power-factor correction and harmonic filtering to improve voltage quality.

Thyristor based rectification has been used commercially to augment existing smelter dc current capability since the 1980s, and only recently have ABB introduced thyristor rectifiers of similar ratings to existing diode equivalents. Similarly, Fuji now offer S-Former (integrated thyristor-transformer) modules, with ratings that also make them attractive alternatives.

While the use of thyristors gives an improvement in dynamic voltage control, it comes at the expense of increased reactive power demand, as reactive power absorption increases in proportion to the sine of the firing-angle. Adding reactive power compensation is a logical but costly solution, and must be rated for full voltage and current. Alternatively, firing-angle can be minimised as is done in HVDC thyristor control by adding OLTCs, but this reintroduces all of the electro-mechanical problems identified earlier, and makes the solution less attractive.

5.1.2 The smelter load

Smelter Pot-lines

Smelting requires extremely large dc currents, often in excess of 320kA, to facilitate the production of commercial quantities of aluminium using the reduction process. The dc load consists of one or more potlines, which in turn are made up of many series connected reduction cells, often in groups of 250 or more. Each cell has a nominal operating voltage which is controlled to around 4.0 - 4.5 V.

The reduction cell is constructed with a movable carbon anode, electrolyte, aluminium cathode, cathode carbon and steel collector as shown in Figure 5.2.

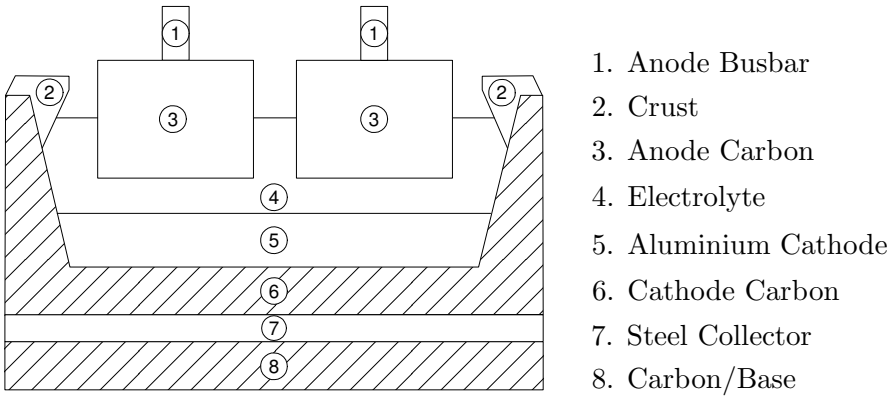


Figure 5.2 Simplified schematic of an aluminium reduction cell

A normal reduction cell production cycle consists of: normal operation, operation for metal tapping (where aluminium is formed near the cathode and syphoned off periodically), alumina feeding, and anode effect quenching. During production, the cell anode is slowly consumed during the process, as are the cell walls, and must be periodically repaired or replaced.

Load profile

Under normal operating conditions the smelter load may be thought of as constant, with voltage and current fluctuations minimised by offsetting each cell's operating cycle within the potline. However, two additional operating conditions, that require increased control flexibility, must also be considered. The first, when a new smelter is commissioned, and the second following a power outage where smelter potlines must be restarted and the cells heated back up to operating temperature.

When a smelter is first commissioned, a small number of new cells are connected and brought up to operating temperature so that their voltages stabilise, with the positions of the other cells in the potline short-circuited. More cells are connected, at a rate of 1 to 2 per day, and as they reach temperature, further cells are added requiring increasing voltage; a process that continues until the full complement is installed. As the series connected cells have a common dc current, current magnitude must be maintained despite the increases in load, otherwise cells may become unstable. A smelter rectifier must therefore be able to supply full rated current from very low voltage to full rated voltage, with continuous control in between. It must also be able to compensate quickly when a new cell is installed, as it may initially be of high resistance, and require a much higher applied voltage across it to maintain potline current flow.

A generic smelter voltage and current profile during commissioning is given in Figure 5.3. The dc current is ramped up in (b), with the minimum number of cells connected, until full rated current is reached, at which point further cells are connected and allowed to reach operating temperature. The small steps in voltage (Figure 5.3(a)) depict the connection of additional cells (from $t = 0.22$ to $t = 1.0$); 10 steps are shown for clarity, but in practice the number of steps will reflect the number of installed cells. The process may be coordinated across several potlines if a common dc supply is used, as applied voltage will also be common.

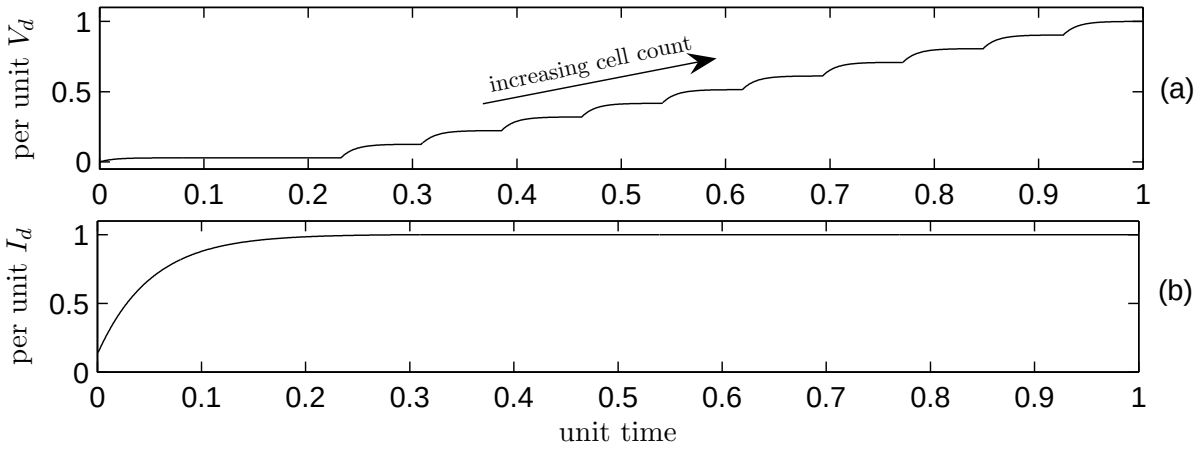


Figure 5.3 Idealised dc voltage and current during smelter commissioning

Once all cells are in service, and full aluminium production has begun, the dc current may again be considered constant, with the voltage varied depending on the number of series connected cells in service. Periodically, some cells are removed for maintenance (to have anode carbon replaced, or cell walls repaired) and their position in the potline is short-circuited. For normal operation at least 90% of the cells are in service, but seldom are all in service at once.

If power is interrupted when a smelter is in full production, the smelter must be promptly restarted before the cells solidify and are made worthless. When the smelter is re-energised, the dc current is brought back up, the rate of increase dependent on how long the cells have been out of service. The current may be increased in several stages to ensure that all cells maintain their voltage balance, although conventional smelters employing tap-changers may not have this flexibility and may instead rely on controllers on each of the individual cells. An example of the smelter response is given in Figure 5.4, the period and step sizes are arbitrary, and are used to illustrate that current rise may be dependent on cell temperature.

This diagram shows that the smelter is restarted (at t=0) with a 10% current order and the current rise is continually monitored. When (at t=0.075) the current level stabilises, the cell temperature is compared to the expected level and when all the cells are within temperature tolerance (shown as label (1) in the Figure) the next stage begins, which is initiated (at t=0.1) with a 70% current order. Once 70% of the current is reached (at t=0.5) and all the cells are

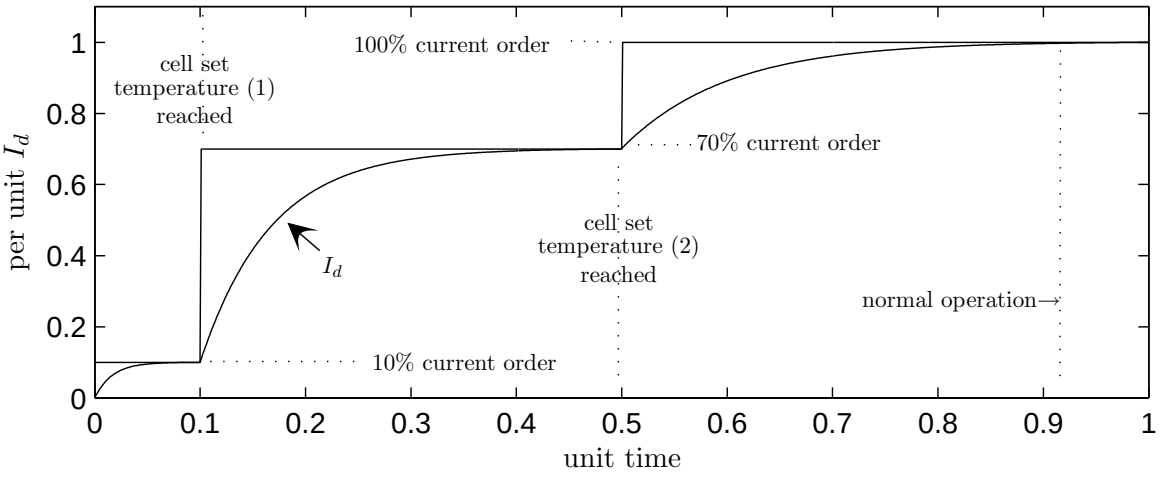


Figure 5.4 Ideal control response during smelter restart

balanced, the 100% current order is given corresponding to full applied dc voltage. At t=0.92, full rated dc current is obtained, and all with cells stabilised at operating temperature, production resumes.

5.1.3 Terminology

In this chapter the basic rectifier unit refers to a six-pulse bridge, the group rectifier unit represents several parallel-connected six-pulse bridges operating under common firing-angle control and the double group two quadrant rectifier refers to two parallel-connected group rectifier units (of any pulse number) operating in two different quadrants and with different firing-angles. The group configurations are paralleled on each of the ac and dc sides. These common connection points are referred to as the ac and dc buses respectively.

5.2 THE PROPOSED CONTROL CONCEPT

Figure 5.5 presents a single line diagram of the proposed double-group two-quadrant configuration. The DC smelter load is represented in the diagram by an inductive (L_d) resistive (R_d) circuit in series with a back emf (V_o) and the total dc current (I_d) is equally divided between the two group rectifier units. The magnitudes of the group ac currents (I_1) and (I_2) are both a function of the dc current and their phase is dependent on the firing angles of their respective groups. Finally, the supply current (I_s) is the vector addition of the two individual ac group currents. If the group firing angles, denoted α_1 and α_2, are selected such that one is leading and the other lagging the common ac terminal voltage (V_T), their imaginary components ($I_1 \sin \alpha_1$)

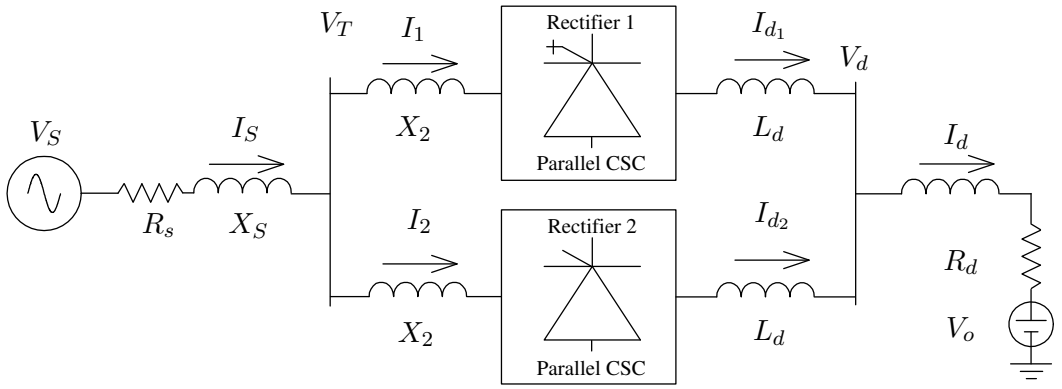


Figure 5.5 Generalised single line diagram of two paralleled rectifiers

and $(-I_2 \sin \alpha_2)$ will cancel out and I_s will be in phase with V_T. The entire controlled rectification process will then appear to the AC system (at V_T) as a resistive load. This operating condition is illustrated in figure 5.6.

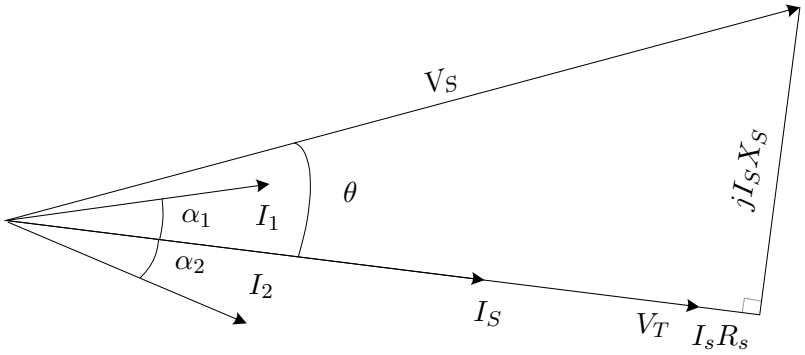


Figure 5.6 Phasor diagram illustrating the case of unity power-factor in a double-group rectifier

5.3 MODEL OF THE PARALLEL-CONNECTED DOUBLE BRIDGE RECTIFIER

A single line diagram of the double-group rectifier is shown in Figure 5.7. Each group rectifier is represented by a single block, though in practice it will be made up of a number of parallel-connected six-pulse rectifier units.

One of the groups (the one with lagging current) can use conventional thyristors, while the other (the one with leading current) must be self-commutating (IGCT-based). The following two subsections analyse the behaviour of this system without (the IGCT case) and with (the thyristor case) commutation overlap.

5.3.1 Without commutation overlap

The circuit equations are derived for one half of the double-group, assuming ideal switching occurs.

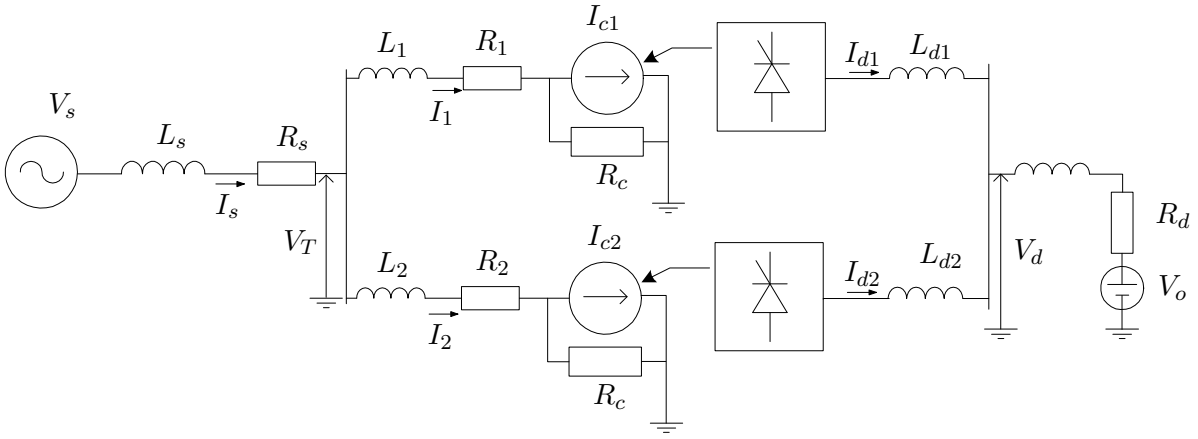


Figure 5.7 Simplified diagram of the hybrid double-group rectifier

At the common ac bus (V_T) the equations for real and reactive power for one group rectifier unit are:

$$P_{T_1} = k_1 V_T I_1 \cos(\alpha_1) \tag{5.1}$$

$$Q_{T_1} = k_1 V_T I_1 \sin(\alpha_1) \tag{5.2}$$

where k_1 is a constant that depends on bridge rectifier configuration and α the firing angle.

Equating powers in terms of dc power (P_d)

$$P_{T_1} - P_{o_1} - P_{l_1} = P_{d1} \tag{5.3}$$

where P_{o_1} is the power loss, and P_{l_1} is the group contribution to the load power.

Given that

$$P_{d1} = V_{d1} I_{d1} \tag{5.4}$$

where

$$V_{d1} = L_1 \frac{dI_{d1}}{dt} \tag{5.5}$$

the combination of (5.3), (5.4) and (5.5) gives

$$L_{d1} I_{d1} \frac{dI_{d1}}{dt} = P_{T_1} - P_{o_1} - P_{l_1} \tag{5.6}$$

and

$$P_{o_1} = (R_{dc} + R_{ac}) I_d^2 \tag{5.7}$$

represents the total group power loss (ac and dc). Equation (5.6) can now be written as

$$\frac{L_{d1}}{2}\frac{d}{dt}I_{d1}^2 + (R_{ac} + R_{dc})I_{d1}^2 = P_{T_1} - P_{L_1} \tag{5.8}$$

Rearranging to make I_{d1}^2 the subject, the equation in the (s) domain becomes:

$$I_{d1}^2(s) = \frac{1}{\frac{L_{d1}}{2}s + (R_{dc} + R_{ac})} \cdot (P_{T_1} - P_{L_1}) \tag{5.9}$$

Equation 5.9 gives the desired output I_{d1} in terms of measured inputs and rectifier parameters. Although the output is in terms of I_{d1}^2 this makes no difference to the control method, and allows the relationship to be considered as linear. No error is introduced as the group rectifier power flow direction and therefore dc current is unidirectional. Thus the above relationships justify the implementation of a linear control system design.

The Thevenin source parameters could be represented in the equations by a suitable D-Q transform similar to [38, 39, 40, 41], from which the terminal voltage could be calculated; however, as parameters L_s and R_s are variable in practice it is better to use the measured terminal voltage directly in the control calculations.

If ideal switches are used and the dc currents between the groups are balanced, the firing angles required to achieve unity power-factor operation will be equal and of opposite polarities and the dc output load voltage will be the average of the contribution from each group rectifier. Their individual contributions for a firing angle of $|15°|$ are given in Figure 5.8(a) and (b) for a leading and lagging angle respectively. The resulting waveform at the common dc bus is given in 5.8(c), and is adapted from [42] for a 6-pulse basic rectifier unit.

From Figure 5.8(c) the upper peaks occur at $-30°$, $30°$, and $90°$ with a maximum value of $\sqrt{2}V_T$, and lower peaks at $0°$ and $60°$ with a value of $\sqrt{\frac{3}{2}}V_T$; valid from $0 \leq |\alpha| \leq 30°$.

Above $|\alpha| = 30°$ the upper peak disappears and $\sqrt{\frac{3}{2}}V_T$ becomes the new peak. A table of the peak values and their valid ranges is given in table 5.1.

Table 5.1 Waveform peaks for varied firing angle (α)

$\lvert\alpha\rvert$	upper peak	lower peak
$0 - 30°$	$\sqrt{2}V_T$	$\sqrt{\frac{3}{2}}V_T$
$30 - 60°$	$\sqrt{\frac{3}{2}}V_T$	$\frac{V_T}{\sqrt{2}}$
$60 - 90°$	$\frac{V_T}{\sqrt{2}}$	0

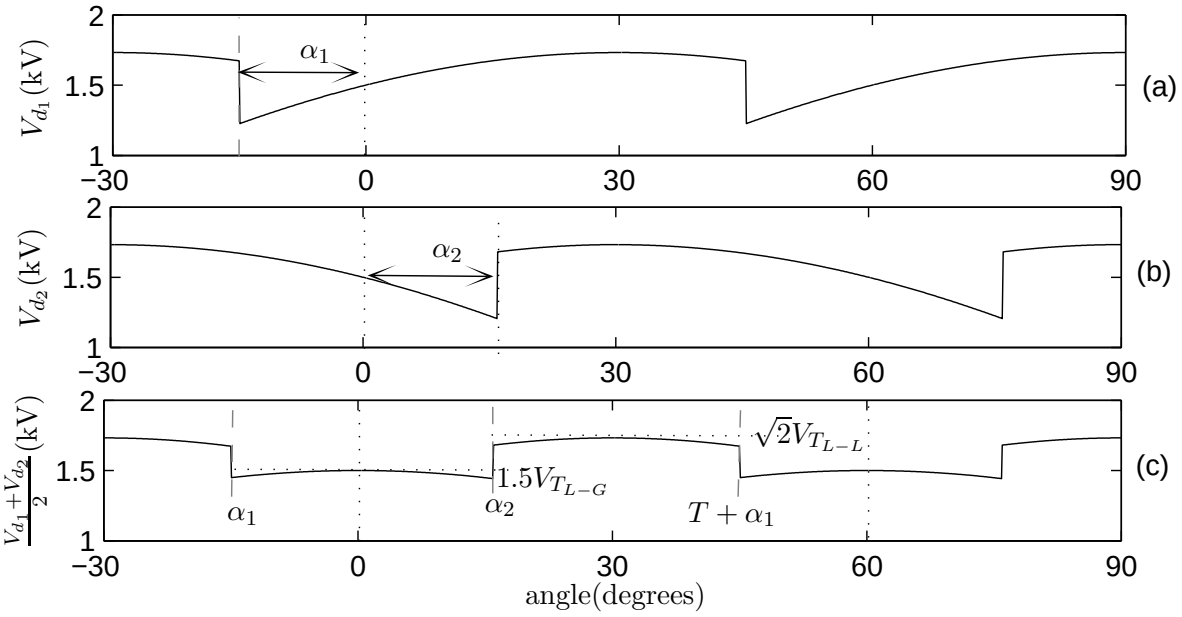


Figure 5.8 Idealised combined dc voltage waveform for 6-pulse paralleled IGCT bridges for a firing angle of $|15°|$

5.3.2 With commutation overlap

To include the effect of the commutation overlap, equations (5.1) and (5.2) are replaced by:

$$P_{th} = 3k_{th}\left(\frac{3\sqrt{2}}{\pi}V_T\cos(\alpha_{th}) - \frac{3I_{d_{th}}X_c}{\pi}\right)I_{d_{th}} \tag{5.10}$$

$$Q_{th} = 3k_{th}\left(\frac{3\sqrt{2}}{\pi}V_T\sin(\alpha_{th}) - \frac{3I_{d_{th}}X_c}{\pi}\right)I_{d_{th}} \tag{5.11}$$

where the subscript $_{th}$ indicates applicability to the thyristor rectifier.

The value of commutation reactance X_c in equations 5.10 and 5.11 is difficult to quantify because it varies with the amount of load connected to the supply system [43].

When comparing the dc output voltage of self commutated and line commutated rectifiers, the differences are most pronounced at small firing angles, where rated current is supplied. In a smelter where both thyristor types are used, the firing angle required for a specified dc voltage will differ between group rectifiers, the exact amount dependent on X_c and I_d.

During the commutation two supply phases are effectively shorted together via their phase impedances, and any other circuit connected to the same terminal will experience the same voltage waveform. This is precisely the case when an IGCT bridge is connected in parallel with

the thyristor bridge as part of the same group; in this case the ac supply voltage will be reduced by the voltage notches caused by the thyristor bridge commutations. The constituent and output dc voltage waveforms of the hybrid Thyristor/IGCT combination are shown in Figure 5.9.

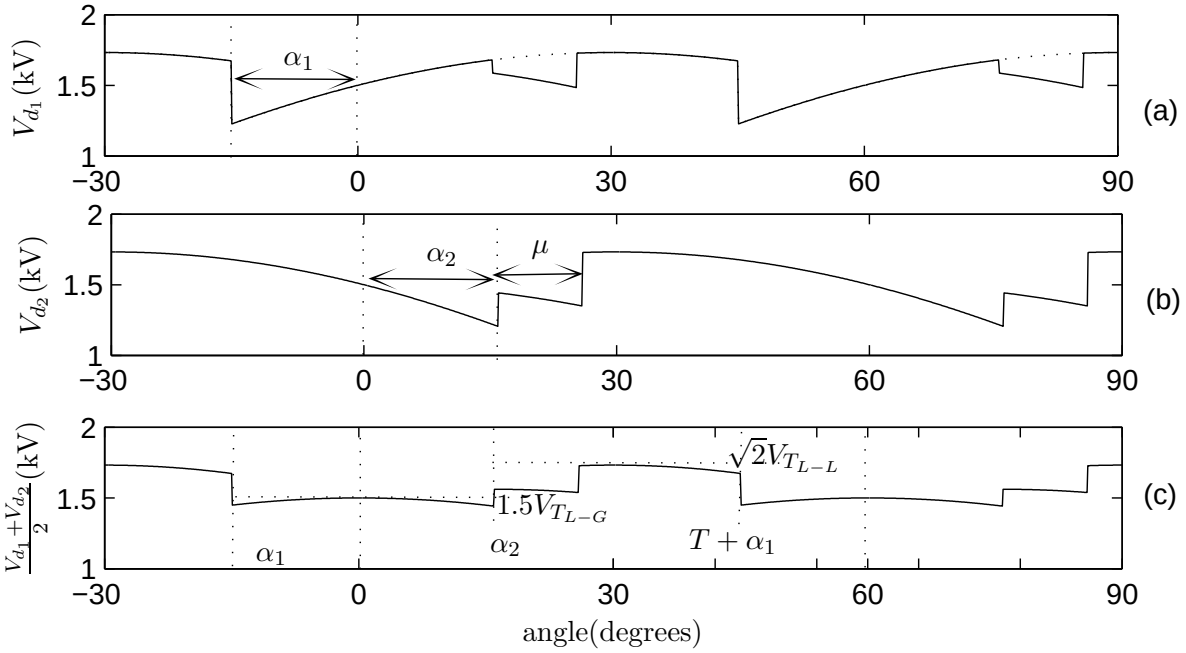


Figure 5.9 Idealised combined dc voltage waveform for 6-pulse paralleled IGCT and thyristor bridges for a firing angle of |15°| and commutation angle of 10°

In Figure 5.9, graph(b) shows the dc output voltage of the thyristor bridge and graph (a) the IGCT bridge voltage. In the latter waveform, the notches caused by the commutation in (b) are evident from 15° to 25°, the dotted line giving the ideal trace. The average dc voltage as seen by the load is given in graph (c), the peak levels of the two sections of the waveforms being $\sqrt{2}V_{T(L-L)}$ and $1.5V_{T(L-G)}$ respectively. Obviously once μ commutation angle delay is greater than angle $(T + \alpha_1)$ the peak values will change, the new peak depending on the magnitude of I_d and X_c.

For equal current sharing to occur, the average dc voltages of the IGCT and thyristor bridges in 5.9(a) and 5.9(b) must be the same under normal balanced operating conditions. Given that in this example the average dc voltage is $1.5250V_{T(L-L)}$ for the thyristor bridge, and higher at $1.5697V_{T(L-L)}$ for the IGCT bridge, equal current sharing would not occur, and so to be feasible, each of the bridges must have differing firing angles. The exact difference depends on the average voltage drop due to the effect of thyristor commutation on each of the bridges.

Although attempts have been made in the literature to analyse and quantify these interactions analytically, the models used have either assumed infinite sources [42] or ideal switchings [44], both questioning the validity of the result. Moreover, even the simplified models require iterative

solutions, which are more suited to computer simulation. This contribution makes no attempt to develop an analytical model and concentrates, instead, on the complete solution that takes the interactions into account in the design of the control system.

5.4 SMELTER APPLICATION

5.4.1 The conventional 48-pulse smelter

Smelting requires extremely large dc currents, often in excess of 320kA, to facilitate the production of commercial quantities of aluminium in potlines using the reduction process. The load current may be split over two or more potlines, which may or may not have dc tie lines between them.

The paralleling of bridges required to get the current rating of the smelter provides the opportunity of phase-shifting their transformers and, thus, increasing the pulse number of the group in multiples of twelve.

The 48-pulse model configuration, shown in Figure 5.10, consists of four phase-shifted twelve-pulse parallel rectifiers, requiring a 7.5° phase-shift between groups as mentioned previously. It can be seen in Figure 5.10 that the transformers have $0 : 30°$ (star-delta) and successive phase-shifts of $7.5 : 37.5°$, $15 : 45°$ and $22.5 : 52.5°$ using zig-zag wound transformers for rectifiers A, B, C, and D respectively.

In conventional smelters employing OLTC and saturable reactors, maintaining an ideal phase-shift was very difficult as even small differences in impedance and the discrete nature of the tap changing mechanism upsetting the 7.5° shift.

5.4.2 The proposed hybrid rectifier

In the proposed hybrid double-group rectifier, shown in Figure 5.10, the provision of a common leading firing command to all the IGCT rectifiers and a common lagging firing angle to all the thyristor rectifiers does not alter the conventional high-pulse operation of the smelter. Likewise, by issuing the same dc current order to the leading and lagging group controllers, the sought after high power-factor is implicitly assured.

At the smelter connection point, the power system is normally weak and this has a major influence on the maximum power transfer and reactive power requirements of the double-group configuration. In the leading group bridges, maximum power is reached when a further increase in current order requires a reduced firing angle, which reduces the reactive power generated and, thus, the ac terminal and dc side voltages; however, the reduction of dc voltage is compensated

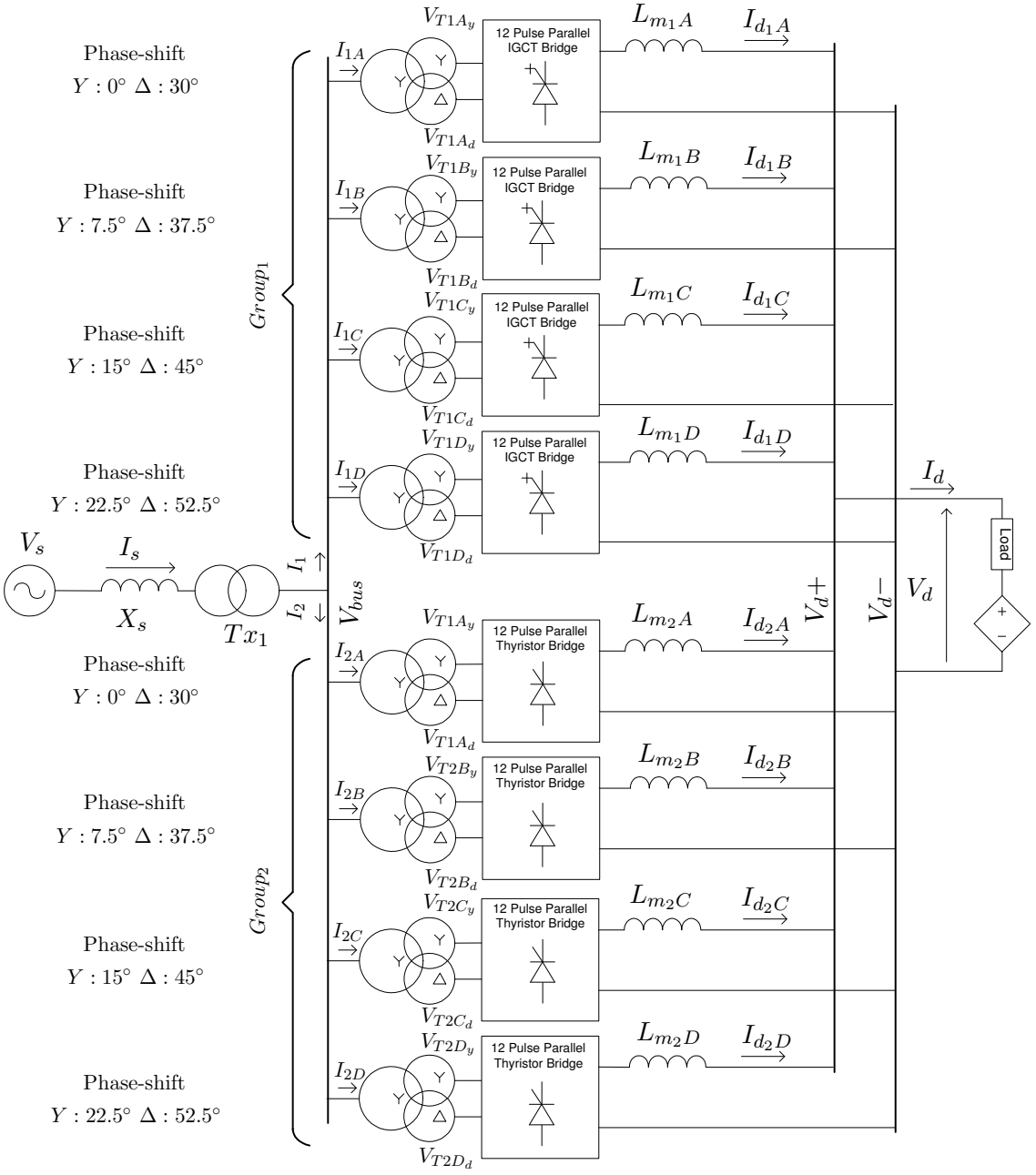


Figure 5.10 Configuration of the hybrid double-group 48-pulse test system

by a further reduction of firing angle, which in turn reduces the reactive power generated and lowers the terminal voltage.

Conversely in the lagging group bridges, a small increase in current order near the rated current (achieved by a reduction of the firing angle), reduces the demand for reactive power increasing V_T and this allows an increase in maximum power transfer. Thus, for some values of firing angle (of the order of 10 to 20°) it should be possible to improve the maximum power output of the

smelter by increasing the current order of the lagging (thyristor based) group and reducing the current order of the leading (IGCT based) group.

5.4.3 Controller Design

The IGCT and thyristor controllers are derived from the circuit equations calculated in section 5.3 and based on the cascaded control block diagram in Figure 5.11. The subscript $_R$ is used to specify that the parameters apply to a generic Group rectifier, and may be replaced by $_1$ or $_2$ for the IGCT and thyristor bridges respectively.

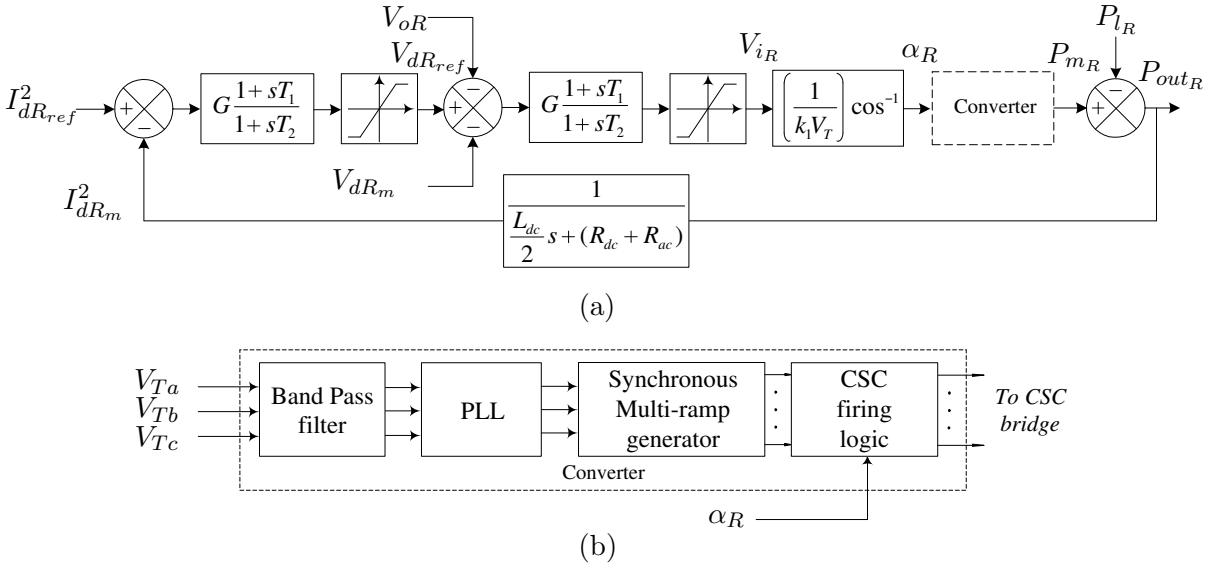


Figure 5.11 Block diagram of the generic smelter controller, with (a) current control and (b) firing angle control

In Figure 5.11(a), current order $I^2_{dR_{ref}}$ is compared to the calculated current $I^2_{dR_m}$ which is itself fed back through a block containing the dc parameters as calculated in (5.8). The resulting current error is passed to a lead-lag compensator whose output defines the voltage control order $V_{dR_{ref}}$. The signal is hard limited to prevent saturation and the difference between it and the measured dc voltage (V_{dR_m}), less the load back emf (V_{oR}), is passed to a second cascaded lead-lag compensator, the output of which defines the incremental voltage (V_{iR}) correction required. V_{iR} is divided by the conversion constant and RMS terminal voltage (k_1V_T) which yields $\cos(\alpha_R)$. The inverse cosine is taken to determine α_R, which is in turn passed to the converter firing logic, as given in Figure 5.11(b).

In the diagram a stable firing angle is developed with reference to the 3-phase terminal voltage, which is band passed and used as the input to the 3-phase phase locked loop (PLL), which in turn is used to generate synchronised ramping control signals for each of the rectifier switches. These ramps are compared to the value of α_R to determine a precise switching pattern.

The same dc voltage must be produced by each rectifier for a given firing angle command, so that dc load current is equally shared between all rectifiers in a group. When the phase is intentionally shifted, as is the case with phase-shifting transformers, the firing angle reference must also be shifted, either with a static increase in angle with respect to the common ac bus, or by physically moving the voltage reference (V_{Ta}, V_{Tb}, V_{Tc} in Figure 5.11(b)) to the low voltage side of the transformer. The latter has the advantage of compensating for changes in ideal shift, but the low voltage waveform is typically more distorted and must be filtered; the filters potentially adding other, variable phase-shifts which must be taken into account.

5.4.4 Component ratings

Ratings for the 6-pulse bridge rectifiers are readily available in the literature and so their proofs will not be reproduced here. Instead a summary of the current ratings for the 6-pulse, 12-pulse and 48-pulse circuits are given below.

Assuming ripple free dc current is supplied equally, the dc load current supplied by each 6-pulse rectifier is:

$$I_{d_{6p}} = \frac{I_d}{n_r n_g} \tag{5.12}$$

where n_r is the number of 6-pulse rectifiers in a group and n_g is the number of groups.

The RMS ac current in each phase of the 6-pulse bridge is

$$I_{6p} = \sqrt{\frac{2}{3}} I_{d_{6p}} \tag{5.13}$$

and the RMS of the fundamental is

$$I_{(1)6p} = \frac{\sqrt{6}}{\pi} I_{d_{6p}} \tag{5.14}$$

for the IGCT case, and

$$I_{(1)6p_{th}} = \frac{\sqrt{6}}{\pi} I_{d_{6p}} \left[\frac{(\cos(2\alpha) - \cos 2(\alpha+\mu))^2 + (2\mu + \sin(2\alpha) - 2\sin(\alpha+\mu))^2}{4\cos(\alpha) - \cos(\alpha+\mu)} \right]^{\frac{1}{2}} \tag{5.15}$$

for the line-commutated thyristor rectifiers as given in [45]. The RMS thyristor and IGCT switch currents are given by

$$I_{sw} = \frac{1}{\sqrt{3}} I_{d_{6p}} \tag{5.16}$$

The rating for the star-delta connected transformer (0° phase-shift) is

$$\text{MVA}_{0^\circ} = 2\frac{V_T}{k_T} I_{d6p} \tag{5.17}$$

where V_T is the RMS voltage of the common ac bus and k_T is the effective rectifier transformer turns ratio.

With multiple windings, the phase-shifting transformer's MVA rating (from [46]) for each secondary (denoted by subscript $_s$) is given as

$$\text{MVA}_{s7.5-22.5} = 0.5 \times \Sigma(V_{w_n} \times I_{d6p}) \tag{5.18}$$

where V_{w_n} is the equivalent sinusoidal RMS voltage of each winding segment, and assuming the two secondary winding sets are of equal rating.

The rating of the phase-shifted transformer primary is thus

$$\text{MVA}_{p7.5-22.5} = \Sigma(V_{w_n} \times I_{d6p}) \tag{5.19}$$

The characteristic 12-pulse current waveform as seen from the primary side of each rectifier transformer is

$$i_{12p}(\omega t) = \frac{4\sqrt{3}}{\pi} I_{d6p} \left(\cos(\omega t) - \frac{1}{11}\cos(11\omega t) + \frac{1}{13}\cos(13\omega t) - \frac{1}{23}\cos(23\omega t) + \frac{1}{25}\cos(25\omega t) - \dots \right) \tag{5.20}$$

Combining all of the 12-pulse phase-shifted current waveforms, the current waveform as seen by the high voltage transformer supplying one group from the ac bus is

$$i_{48p}(\omega t) = \frac{16\sqrt{3}}{\pi} I_{d6p} \left(\cos(\omega t) - \frac{1}{47}\cos(37\omega t) + \frac{1}{49}\cos(49\omega t) - \frac{1}{95}\cos(95\omega t) + \frac{1}{97}\cos(97\omega t) - \dots \right) \tag{5.21}$$

the rms fundamental current for one 48-pulse group is thus

$$I_{48p} = \frac{8\sqrt{6}}{\pi} I_{d6p} \tag{5.22}$$

and when two groups are combined

$$I_{s_{48p}} = \frac{16\sqrt{6}}{\pi} I_{d6p}$$

which is written in terms of the total dc load current (I_d) as

$$I_{s_{48p}} = \frac{2\sqrt{6}}{\pi} I_d \tag{5.23}$$

The phase of each of the harmonic components in (5.21) will vary with firing angle and when two groups are combined their characteristic harmonics will either be attenuated or amplified for certain values of firing angle.

Finally, the MVA rating of the supply transformer (Tx_1 from Figure 5.10) with respect to the common ac bus is

$$\text{MVA}_{Tx_1} = V_T \times I_{s_{48p}} \tag{5.24}$$

5.5 SIMULATED PERFORMANCE OF THE TWO-QUADRANT CONTROLLED SMELTER

5.5.1 Test system

The test system is a 300 MW smelter consisting of two group rectifiers, each made up of four twelve-pulse equivalent rectifiers in the configuration shown in Figure 5.10.

Only one potline is used, with a nominal dc voltage of 1 kV with the applied voltage and back emf of the individual cells being 4 V and 1.7 V respectively. Therefore to emulate the full smelter, 250 cells need to be placed in series. As shown in Figure 5.7, the test system also includes a load resistance (calculated to provide the full 320 kA load capacity at full voltage) and a lumped inductance (representing all the dc side inductances). Alternative models [47][48] have been used in the literature to model the potline.

The incoming supply is represented by a Thevenin equivalent with V_s and X_s set to 220 kV and 0.17 H respectively, providing an SCR of approximately 3. Transformer T_{X1} supplies 33 kV to the common bus that feeds the rectifier transformers and has a leakage reactance of 10%.

Each rectifier within a group is supplied by a phase-shifted transformer, providing conversion from 33 kV to 0.8 kV AC as input to the rectifier bridges, with leakage reactances for each specified as 5%.

The dc outputs are paralleled through small intergroup reactors ($L_{m1A}-L_{m1D}$ and $L_{m2A}-L_{m2D}$) which allow for instantaneous differences between each of the dc connections. The rectified dc voltage outputs from these groups range from 0 to a maximum (unloaded) of 1100 Vdc.

The dc load is represented by a resistance and back emf of $1.5m\Omega$ and 420 V respectively, with V_d and I_d representing the load dc voltage and current measurements.

The dc side circuit parameters are in practice reasonably constant during normal operation, but they vary greatly during the cell warm up phase. The temperature characteristics of the cells are well known and, thus, by monitoring the cell temperature during this operating phase the nominal controller gains can be adjusted, or alternatively the gain can be scheduled to ensure stable voltage and current control.

5.5.2 Dynamic response

The test system has been modelled in PSCAD/EMTDC and the response to a series of current step changes recorded over a 24 second period, a time scale much shorter than would be the case in practice; this is done to enable the computer solution in a realistic time; consequently the dc inductances are reduced by a factor of ten to produce a realistic di/dt . The solution period includes commissioning, normal operation, cell maintenance and shut down phases, as well as a restart under current control. The shut down phase constitutes a controlled reduction in dc load current, as opposed to the interruption of power when the ac circuit breakers are opened.

The Smelter response is given in Figure 5.12. At time $t = 0.1s$, commissioning begins, with initially 20% of the cells connected and the remaining positions in the potline short-circuited. The smelter is energised with a 10% current order as given in Figure 5.12(b) which is then increased to 100% at $t = 1s$. 90% current is reached at $t = 5s$ where additional cells are connected. Subsequent cells are installed at $0.5s$ intervals until all are in service at $t = 8s$. The dc voltage and real power traces increase as expected in Figures 5.12(a) and (b) respectively. Negligible change is observed in I_d and Q_T, with high power-factor maintained throughout.

At $t = 9s$, 10% of the installed cells are shorted to simulate their removal for maintenance, the dc voltage as observed in Figure 5.12(c) decreases to maintain I_d constant as does the real power in Figure 5.12(a). The cell removal requires a reduction of the applied dc voltage in order to maintain the current constant. The dc voltage reduction requires an increase of the absolute firing angle and, thus, an increase in reactive power absorption in the thyristor group and an increase in reactive power generation in the IGCT group, such that the net reactive power at the smelter terminals remains practically unchanged. The removed cells are reinstated at $t = 10s$.

At $t = 12s$ the shut-down command is given and the controlled reduction of I_d begins. The current is first ramped down at a rate limited to 60kA per second to prevent excessive reactive power circulation. When half power is reached the ramp rate is increased to 120kA per second, until the real power flow ceases (at 14 s) and the remaining current flow decays to zero (at t=14.7 s). The HV supply circuit breakers are then opened.

Smelter restart begins at $t = 15s$ where a 64 kA (20%) current order is given, followed by a 225kA (70%) order at 16.25 s, and finally a 320 kA (100%) current order at 18.25 s, with normal

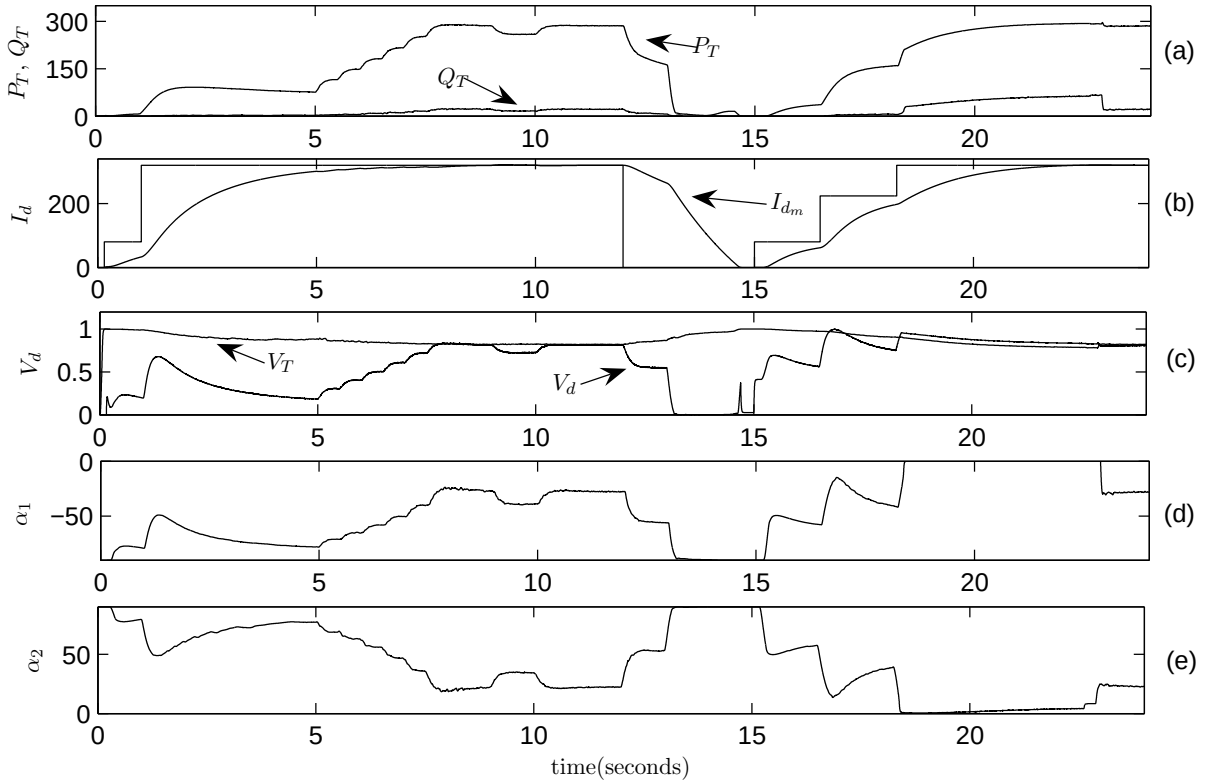


Figure 5.12 Simulated smelter performance, with (a) real and reactive powers, (b) ordered and measured dc currents, (c) normalised dc voltage and terminal voltage, (d) leading firing angles, (e) lagging firing angles

operation recommencing at approximately 23 seconds.

The active and reactive power responses on the high voltage side of the supply transformer (T_{x1}) are shown in Figure 5.12(a). The lagging and leading reactive power contributions are shown in Figures 5.13(a) and (b) respectively. High power-factor operation is seen to be maintained (Figure 5.13(c)), with an average of 0.999 observed during normal operation and dropping briefly to 0.976 during restart (at about t=22.8 s); this is due to the reactive power demands of all transformers when the rectifiers operate at zero firing angle.

5.5.3 Waveform quality

The high quality of the full load current waveform (I_s) at the smelter supply, shown in Figure 5.14(a), is clearly evident.

Due to the lack of commutation overlap, the stepped 48-pulse waveform is more obvious in the case of the IGCT (shown in Figure 5.14(b)). The corresponding harmonic spectra of the supply current, shown in Figure 5.15, indicates levels of 1.6% for the 47th, 49th, 0.99 for the 95th, 97th and 0.6% for the 143rd, 145th characteristic harmonics, the Total Harmonic Distortion being

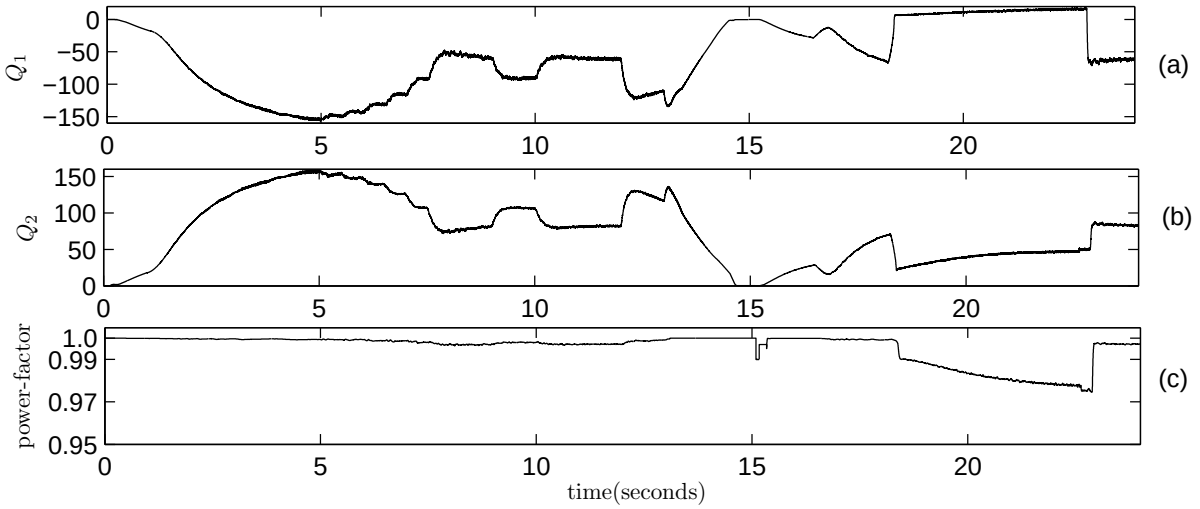


Figure 5.13 Smelter reactive power circulation with (a) generation in group 1, (b) absorption in group 2 and (c) power-factor as seen from the smelter terminal

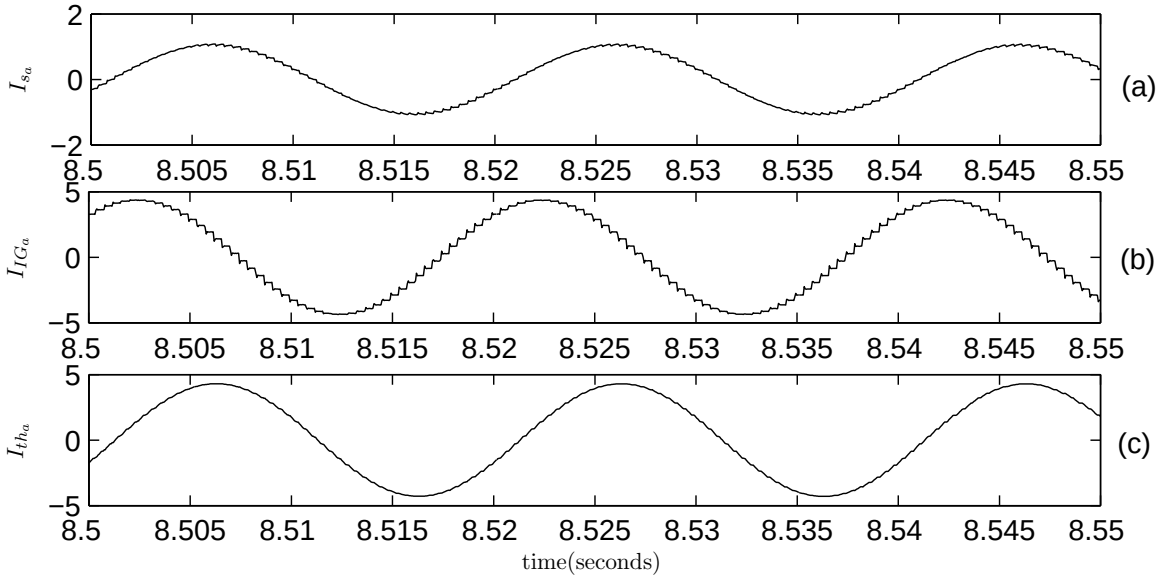


Figure 5.14 Ac currents for the entire smelter in (a), combined IGCT bridges in (b) and thyristor bridges in (c)

2.63%.

5.6 48 PULSE OPERATION WITH CENTRE-TAPPED RECTIFIERS

A potential improvement to the IGCT-Thyristor rectifier detailed in Section 5.5 is the replacement of the transformers and rectifier bridge circuits for each 6-pulse rectifier with a centre-tapped configuration. The immediate advantage of this is the reduction in switching losses as

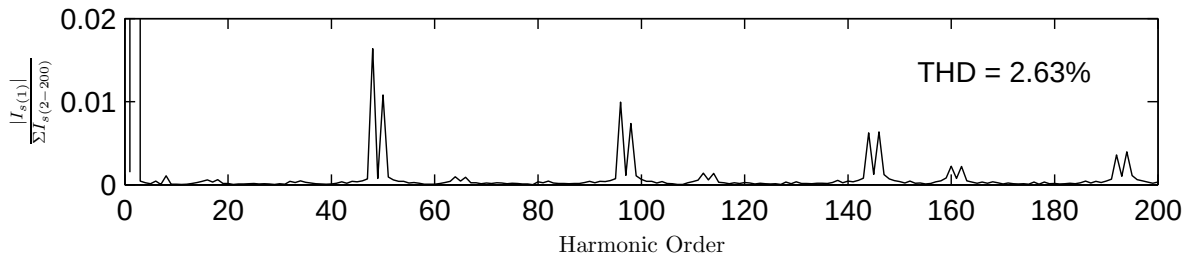


Figure 5.15 Harmonic performance of supply current (I_s) for the first 200 Harmonic orders, as taken from one cycle of Figure 5.14 (a)

only one thyristor conducts at any given time. Each thyristor only conducts for 60° of a cycle, as opposed to 120° for the bridge configuration, meaning the average thyristor dc current is half for the same rectifier power rating. The traditional argument for the use of the bridge configuration is a better utilisation of the rectifier transformer, whereby the secondary windings conduct in both directions. This is further justified by the need to connect switches in series to provide the voltage ratings required in medium and high voltage applications. However, the latter argument does not apply to the smelter case, where the dc voltage (below 2 kV) can be obtained with a single switch. Moreover, while the secondary transformer windings are simpler in the bridge configuration, especially when phase-shifting is considered, it is at the expense of doubling their average current rating, which is a limiting factor in the design of the smelter transformers. The number of switches remains the same (six), each rated at double voltage and half average current. A consideration with the six-phase connection is that the primary winding must be delta connected to permit triplen harmonic current circulation [43], and must be sufficiently rated.

5.6.1 Component Ratings

The rectifier thyristors conduct individually for 60°, their ratings in relation to the dc current of one 6-pulse rectifier ($I_{d_{6p}}$) is given below, following on from equation 5.12.

The RMS ac current in each phase and therefore each of the thyristor and IGCT switches in the 6-phase rectifier is

$$I_{6phase} = \frac{1}{\sqrt{6}} I_{d_{6p}} \tag{5.25}$$

and the RMS of the fundamental is

$$I_{(1)6phase} = \frac{\sqrt{3}}{\pi} I_{d_{6p}} \tag{5.26}$$

for the IGCT case, and

$$I_{(1)6phase_{th}} = \frac{\sqrt{3}}{\pi} I_{d_{6p}} \left[\frac{(\cos(2\alpha) - \cos 2(\alpha+\mu))^2 + (2\mu + \sin(2\alpha) - 2\sin(\alpha+\mu))^2}{4\cos(\alpha) - \cos(\alpha+\mu)} \right]^{\frac{1}{2}} \tag{5.27}$$

for the line-commutated thyristor rectifiers.

With series connected phase-shifted windings, the transformer's MVA rating for each secondary (denoted by subscript $_s$) is given as

$$\text{MVA}_{s7.5-22.5} = 0.5 \times \Sigma(V_{w_n} \times I_{d6p}) \tag{5.28}$$

where V_{w_n} is the equivalent sinusoidal RMS voltage of each winding segment, and assuming the two secondary winding sets are of equal rating.

The rating of the 12-pulse primary connection with two 6-phase secondary windings is a combination of the RMS values of each of the secondary ac currents.

$$\text{MVA}_{0^\circ} = 2\frac{V_T}{k_T} I_{d6p} \tag{5.29}$$

where V_T is the RMS voltage of the common ac bus and k_T is the effective rectifier transformer turns ratio. This is, as expected the same as equation 5.17 for the bridge rectifier case. The characteristic harmonics, group current rating and supply transformer MVA rating are thus the same as in equations 5.20 to 5.24.

5.7 CONCLUSIONS

A Thyristor/IGCT double-group 48-pulse rectifier that provides two-quadrant power controllability has been described and its performance for the control of a 320 kA aluminium smelter tested via extensive PSCAD/EMTDC simulation.

The proposed system provides high power-factor throughout the operating cycle without the assistance of reactive power compensation and transformer on-load tap-changers, while maintaining the traditional high-pulse ac-dc conversion. The results have shown the ability of the proposed system to provide flexible full range control and fast dynamic response during commissioning, normal operation, shut-down and smelter restart.

With the increasing current rates of the thyristor-based self-commutating switches the proposed configuration should be a viable competitor to the present technology used by the aluminium smelting industry.

Chapter 6

HIGH-CURRENT TWO-QUADRANT MULTILEVEL CURRENT REINJECTION

6.1 INTRODUCTION

Large scale dc supplies are used throughout industry with current ratings of 10 kA to 500 kA for the metal processing and refining of copper, zinc, manganese, steel and aluminium, and in the production of chemicals such as chlorine, with plants rated from 10 to 100 kA. The dc current is typically delivered using a combination of on-load tap-changing (OLTC) transformers and diode rectifiers, with the largest units using parallel connected phase-shifted transformers to increase harmonic performance.

High pulse operation using phase-shifting methods is uneconomical for other than very large power rating applications, due to the large number of complex secondary connections required (i.e. 48-pulse operation requires eight 3-phase secondaries). So, instead, use is made of harmonic filters and power-factor correction, which although costly, are required to meet supply quality regulations. When converters are fed via weak transmission systems, additional compensation may be required to support the ac terminal voltage; interaction between the system and harmonic filters in this case potentially causing instability, with parallel resonances at low order harmonics.

Reactive power demand in traditional high current installations is minimised by using OLTC and reactive power compensation, a method still used with high current line commutated thyristor based dc rectifiers. Some improved configurations have been proposed [49, 50, 51] for specific applications; however, for acceptable harmonic performance they require either equal dc current sharing (in the case of the parallel-connected rectifiers), suffer additional switching losses (in the case of PWM control) or they are series-connected, all of which are far from ideal.

In Chapters 2 and 4, the series-connected MLCR has been presented as a viable alternative to conventional line-commutated HVDC transmission. While high power operation and flexible reactive power control are possible with this topology, it is not well suited to high current applications due to the large number of switches in the conduction path at any one time. The

parallel MLCR scheme (the basic structure summarised in Appendix A) however has half the number of series connected switches, while offering similar benefits and flexibility. Moreover, in the multi-level reinjection configuration, high-pulse operation is achieved without the need for phase-shifting transformers irrespective of the number of rectifiers that are in operation.

This Chapter summarises the development of a generalised modular high pulse ac-dc rectifier topology capable of delivering very high dc current with flexible, high power-factor operation.

6.2 THE TWO-QUADRANT CONTROL CONCEPT

Although a single MLCR rectifier is capable of developing the required pulse number (48 in the 5-level case), the current capacities of potential applications may require several MLCR rectifiers connected in parallel. By pairing up individual rectifiers, one with a leading and the other with a lagging firing angle, high power factor operation is possible, and the dc current capability is increased. Potential applications include chlorine production plants, where dc currents are in excess of 40 kA and high pulse number is desired, but is uneconomical or impractical with conventional phase-shifted rectifier topologies. Likewise copper electro-winning is performed at currents of 10-100 kA [52] and a number of MLCR high power-factor lead/lag pairs could be parallel connected to achieve the required current levels. Other industrial processes including the production of manganese, magnesium, zinc and steel, require similar magnitude dc currents, but the largest dc current requirements come from the aluminium smelting industry where 500 kA is possible [53], with several pairs of rectifier units in parallel. The MLCR rectifiers have

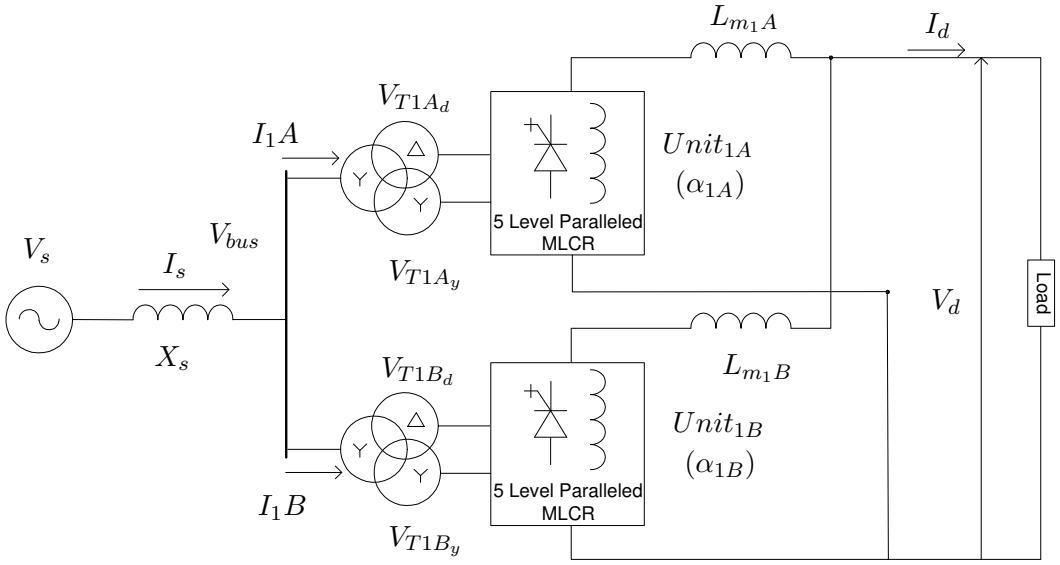


Figure 6.1 Rectifier group consisting of two paralleled 5-Level 48-pulse MLCR rectifiers

more switches in the conduction path at a given instant, as compared to conventional bridge

rectifiers, but they use much simpler and efficient transformer connections. With MLCR 48-pulse operation is possible using a single star-delta/star transformer as opposed to eight conventional phase-shifted secondaries if suitable transformer secondary ratings are available.

Figure 6.1 shows the block diagram of two MLCR units (A and B) that are connected in parallel on both the DC and AC sides. The AC system beyond the common ac bus (V_{bus}) is represented by a Thevenin equivalent (V_S and X_S). On the low voltage side of the transformers the ac voltages are V_{T1A} and V_{T1B} with further subscripts $_d$ and $_y$ used to indicate the delta and star connections respectively. On the DC side, small intra-group reactors (L_{m_1A} and L_{m_1B}) are used to allow the parallel connection despite the instantaneous voltage mismatches.

Unlike traditional thyristor rectifiers, the MLCR switch commutation is performed under zero current, and the conventional reduction in dc voltage due to thyristor commutation is absent. The leading-lagging combination of Figure 6.1 should therefore produce the same average dc voltage for a given firing angle regardless of polarity.

The MLCR current waveforms in each of the supply transformer secondary windings are time varying functions. The quasi-sinusoid developed on the transformer primary side has the effect of phase-shifting the secondary transformer terminal voltage relative to the primary winding voltage across the complex impedance of the transformer. The magnitude and phase of the shift are dependent on the ac current magnitude, transformer leakage reactance and firing angle. A phasor representation for a leading and lagging firing angle is given in Figure 6.2.

Figure 6.2(a), the leading case, shows the increased terminal voltage relative to the common bus voltage; conversely a decrease in 6.2(b) is observed for a lagging firing angle.

When connected in parallel, the relationship between leading and lagging rectifier terminal voltages ($V_{T_{1A}}$ and $V_{T_{1B}}$ respectively) and the common dc voltage is

$$V_d = k_m V_{T_{1A}} \cos(\alpha_{1A}) = k_m V_{T_{1B}} \cos(\alpha_{1B}) \tag{6.1}$$

where k_m is the conversion constant which is dependent on topology, and the firing angles are referenced to each of the rectifier terminal voltages.

With reference to Figure 6.2, the relationship between the terminal voltage (V_T) and bus voltage (V_{bus}) is

$$V_{bus}^2 - V_T^2 = I^2X^2 - 2IXV_T \sin(\alpha) \tag{6.2}$$

Rearranging (6.2) to isolate V_T yields

$$V_T = -IX \sin(\alpha) \pm \sqrt{V_{bus}^2 - I^2X^2 \cos^2(\alpha)} \tag{6.3}$$

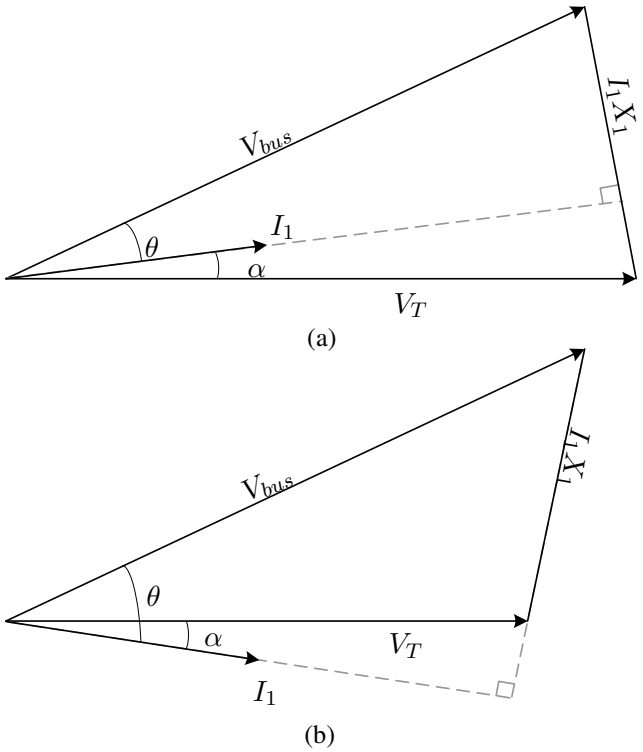


Figure 6.2 Operation of a single rectifier group for a leading (a) and lagging (b) firing angles

which when combined with equation (6.3) with respect to rectifier $1A$ becomes

$$V_d = k_m \cos(\alpha_{1A})(\sqrt{V_{bus}^2 - I_{1A}^2 X_{1A}^2 \cos^2(\alpha_{1A})} - I_{1A} X_{1A} \sin(\alpha_{1A})) \tag{6.4}$$

The absolute values of firing angles α_{1A} and α_{1B} are dependent on the terminal voltages $V_{T_{1A}}$ and $V_{T_{1B}}$ respectively, which are in turn dependent on their ac current magnitude and angle and the resulting complex voltage across each of the rectifier transformer leakage reactances.

If the ac bus is supplied via a series impedance as in Figure 6.1, the ac bus voltage becomes a function of each rectifier's ac current and firing angle, making the system response very non-linear.

6.2.1 AC system analysis

The ac supply current waveform of the parallel MLCR (as given in Figure A.2 of Appendix A)is a combination of each of the thyristor rectifiers' and the reinjection circuit supply currents. A Fourier analysis is performed to find the expected peak, RMS and total harmonic distortion (THD) of the combined current. The analysis is carried out under ideal conditions, with constant I_d, to simplify the solution.

The solution for an m level MLCR bridge is next summarised, with a full proof available in [54].

Currents drawn by each of the star and delta bridges are found as follows:

The star connected bridge contribution to the supply current is

$$\begin{aligned} I_{aYn} &= \frac{2}{\pi}\int_0^{\pi} I_{aY}(\omega t)\sin(n\omega t)d(\omega t) \\ &= \frac{8[1-(-1)^n]I_d}{n\pi(m-1)}\sin\left(\frac{n\pi}{12(m-1)}\right)\cos\left(\frac{n\pi}{6}\right)S_{An} \\ &\quad for\ m \geq 3,\ n = 1,2,3,\cdots \end{aligned} \tag{6.5}$$

and that of the delta connection

$$\begin{aligned} I_{ca\Delta n} &= \frac{2}{\pi}\int_0^{\pi} I_{ca\Delta}(\omega t)\sin(n\omega t)d(\omega t) \\ &= \frac{8[1-(-1)^n]I_d}{3n\pi(m-1)}\sin\left(\frac{n\pi}{12(m-1)}\right)\cos\left(\frac{n\pi}{6}\right)S_{Bn} \\ &\quad for\ m \geq 3,\ n = 1,2,3,\cdots \end{aligned} \tag{6.6}$$

where

$$\begin{aligned} S_{An} &= (m-1)\sin\left(\frac{n\pi}{6}\right) + \sum_{i=1}^{m-2} i\sin\left(\frac{n\pi}{3} + \frac{in\pi}{6(m-1)}\right) \\ S_{Bn} &= (m-1)\sin\left(\frac{n\pi}{3}\right) + 2\sum_{i=1}^{m-2} i\cos\left(\frac{n\pi}{6}\right)\sin\left(\frac{n\pi}{3} + \frac{in\pi}{6(m-1)}\right) \end{aligned}$$

The total bridge supply current $I_{a_R}(\omega t)$ is found by combining equations 6.5 and 6.6, giving:

$$I_{a_R}(\omega t) = \frac{1}{k_n}[I_{aY}(\omega t) + \sqrt{3}I_{ca\Delta}(\omega t)] \tag{6.7}$$

where k_n is the interface transformer turns ratio. The Fourier components of $I_{a_R}(\omega t)$ are

$$I_{a_Rn} = \frac{8[1-(-1)^n]I_d}{\sqrt{3}k_n n\pi(m-1)}S_{Cn}S_{Dn} \quad for\ m \geq 3,\ n = 1,2,3,\cdots \tag{6.8}$$

where

$$\begin{aligned} S_{Cn} &= \sin\left(\frac{n\pi}{12(m-1)}\right)\cos\left(\frac{n\pi}{6}\right) \\ S_{Dn} &= 2(\cos\left(\frac{n\pi}{6}\right) + \frac{\sqrt{3}}{2})S_{An} \end{aligned}$$

The fundamental peak value of the parallel MLCR bridge output current, derived from Equa-

tion 6.8 is

$$I_{a_R1} = \frac{16\sqrt{3}I_d}{k_n\pi(m-1)} \sin\left(\frac{\pi}{12(m-1)}\right)\left[\frac{(m-1)}{2} + \sum_{i=1}^{m-2} i\cos\left(\frac{\pi}{6} - \frac{i\pi}{6(m-1)}\right)\right] \tag{6.9}$$

The output RMS line current of the bridge is thus:

$$\begin{aligned} I_{a_Rrms} &= \sqrt{\frac{1}{\pi}\int_0^{\pi} I_A(\omega t)^2 d(\omega t)} \\ &= \frac{\sqrt{4+\sqrt{3}}}{3k_n} I_d \sqrt{1 + \frac{11-6\sqrt{3}}{13(m-1)^2}} \end{aligned} \tag{6.10}$$

Given that a 5-level, 48-pulse MLCR bridge is used throughout this chapter, equations 6.8 and 6.10 can be simplified for $m = 5$ so that:

$$I_{a_R1} = \frac{1.7063}{k_n} I_d \tag{6.11}$$

$$I_{a_Rrms} = \frac{0.8}{k_n} I_d \tag{6.12}$$

The Total Harmonic Distortion (THD) of the output current for the 5-level configuration is

$$THD_{I_{aR}} = \sqrt{\frac{2I_{a_Rrms}}{I_{a_R1}^2} - 1} \ = 4.00\% \tag{6.13}$$

6.2.2 Component ratings

Simplified ratings are calculated based on the reinjection bridge being directly connected to an ideal source and under steady state operation. The rated supply current is specified as $I_{a_{rated}}$ and taken from the fundamental current $I_{a_R(1)}$. The following calculations apply to the 5-level ($m = 5$) MLCR.

Supply transformer

The MVA rating of the supply transformer is

$$S = 3V_{T_{rated}} I_{a_{rated}} \tag{6.14}$$

where $V_{T_{rated}}$ and $I_{a_{rated}}$ are the rated fundamental RMS phase voltage and line current of the supply transformer primary. The fundamental component of the output current I_{a_R} is the

rectifier system rated current $I_{a_{rated}}$.

From (6.9), the rated current $I_{a_{rated}}$ is expressed as

$$I_{a_{rated}} = k_i \cdot I_d \tag{6.15}$$

where

$$k_i = \frac{\sqrt{6}(2-\sqrt{3})}{4k_n\pi\sin(\frac{\pi}{48})} \tag{6.16}$$

The supply transformer primary voltage rating is taken as V_T, with the star and delta secondaries rated at $\frac{V_T}{k_R}$ and $\frac{\sqrt{3}V_T}{k_R}$ respectively.

Similarly the transformer phase current RMS ratings are tabulated below:

Y primary $\quad I_{a_{rms}} = \dfrac{\sqrt{4+\sqrt{3}}}{3k_nk_i}\sqrt{1+\dfrac{11-6\sqrt{3}}{52}}I_{a_Rrated}$

Y secondary $\quad I_{aY_{rms}} = \dfrac{\sqrt{2+(4)^{-2}}}{3k_i}I_{a_Rrated}$

Δ secondary $\quad I_{ca\Delta_{rms}} = \dfrac{\sqrt{2+(4)^{-2}}}{3\sqrt{3}k_i}I_{a_Rrated}$

The fundamental (RMS) component of the phase currents are given as:

Y primary $\quad I_{a_{R(1)}rms} = I_{a_Rrated}$

Y secondary $\quad I_{aY_{R(1)}rms} = \dfrac{k_nI_{a_Rrated}}{2}$

Δ secondary $\quad I_{ca\Delta_{R(1)}rms} = \dfrac{k_nI_{a_Rrated}}{2\sqrt{3}}$

Multi-tapped reactor

The operating frequency of the 48-pulse MLCR reactor is 6 times the supply frequency.

The phase voltage RMS rating (with reference to Figure A.1) is found as:

$$\begin{aligned} &= \sqrt{2}k_n^{-1}V_T\sin\left(\frac{\pi}{12}\right)\sqrt{2-\frac{6}{\pi}\cos(2\alpha_R)} \\ &= \sqrt{6}k_n^{-1}\sin\left(\frac{\pi}{12}\right)\sqrt{2+\frac{6}{\pi}}V_{T_{rated}} \end{aligned}$$

As the turns ratio of each of the reactor windings is equal, the proportion of the dc current is shared across them, with $\frac{3}{4}I_d$ across the first and 4^{th} windings, and half I_d across windings 2 and 3.

The RMS current rating of a four winding reactor is generalised as:

$$\begin{aligned} & \sqrt{\frac{1}{4}\sum_{i=1}^{3}\left[\frac{iI_d}{4}\right]^2} \\ = \quad & \frac{\sqrt{21}}{4}I_d \\ = \quad & \frac{\sqrt{21}}{4k_i}I_{a_R rated} \end{aligned}$$

Switching devices

The voltage rating (forward/reverse) of the main bridge switches is

$$V_{sw} = \sqrt{6}k_n^{-1}V_{T_R rated}$$

The RMS current rating of each of the main bridge switches is

$$I_{sw_{rms}} = \frac{\sqrt{2+4^{-2}}}{3\sqrt{2}k_i}I_{a_R rated}$$

The RMS current rating for the reinjection switches S_{j1} and S_{jm} is

$$I_{jsw_{rms}} = \frac{I_{a_R rated}}{k_i 2\sqrt{2}}$$

and for the all other reinjection switches

$$I_{jsw_{rms}} = \frac{I_{a_R rated}}{2k_i}$$

The maximum voltage (forward/reverse) a reinjection switch is subjected to occurs when either switch 1 (S_{j1}) or switch 5 (S_{j5}) conducts. In an m level rectifier, if S_{jm} conducts, the general expression for the voltage across the k^{th} reinjection switch, S_{jk} is

$$V_{S_{jk}} = \frac{(5-k)}{4}V_M \qquad k = 1, 2, 3...m$$

and

$$max\left[V_{S_{jk}}\right] = \frac{2\sqrt{6}k_n^{-1}(m-k)}{(m-1)}\sin\left(\frac{\pi}{12}\right)V_{SR}$$

Therefore the voltage rating of the reinjection switches in a 5-level MLCR is

$$V_{jsw} = 2\sqrt{6}k_n^{-1}\sin\left(\frac{\pi}{12}\right)V_{SR}$$

6.3 THE MULTI-GROUP MLCR RECTIFIER

In very high-current applications several MLCR rectifier groups are parallel connected on the ac and dc sides to form a multi-group configuration. Figure 6.3 presents an 'n' group MLCR scheme, with each of the rectifiers connected to a common medium voltage ac bus (V_{bus}). The transformers, rectifiers and smoothing reactors are of identical rating and construction.

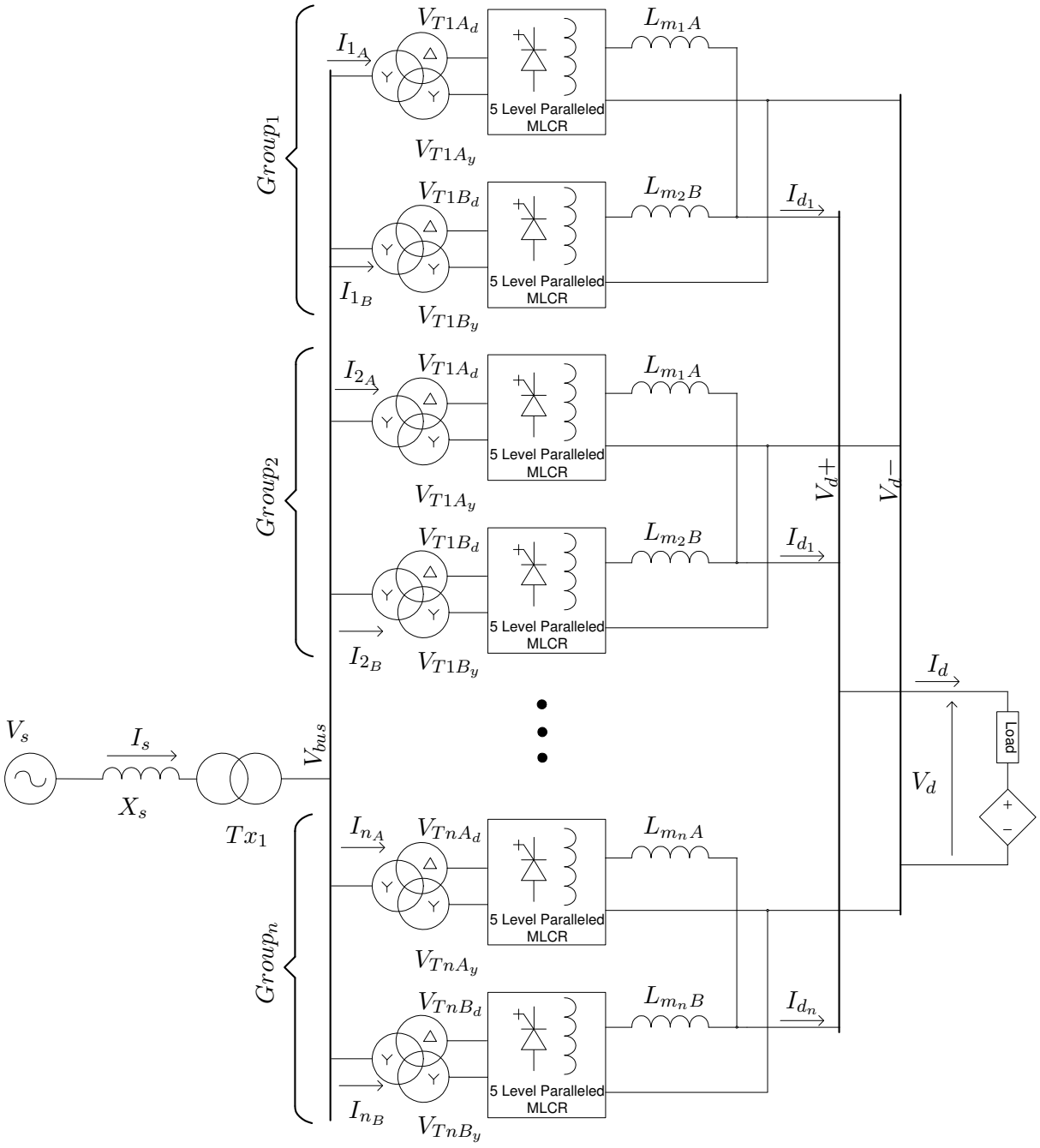


Figure 6.3 Paralleled test system comprised of 'n' groups

As each group constitutes a 5-level high power-factor rectifier, harmonic performance is assured regardless of the current contributions of each rectifier. Moreover, as long as the dc current is balanced between the leading and lagging rectifiers in a group, high power factor is maintained. Therefore, unlike traditional phase-shifted high-pulse rectification, each rectifier's dc current may be controlled directly and independently. As a consequence, the dc side parallel connections are greatly simplified, and are made without the need for interphase reactors, a limitation of traditional high-pulse phase-shifted transformer rectifiers.

6.3.1 Independent Group current control

Independent dc current control also affords a rectifier group with increased flexibility. If power ratings allow, the current may be deliberately increased in the leading or lagging rectifier to change the phase of the group supply current (e.g. I_1 in Figure 6.3) relative to the bus voltage (V_{bus}), providing additional, but limited power-factor control. Generating a surplus of reactive power has the potential to correct for other inductive loads on the common connection (such as transformer reactances and induction machines), or to export back to the system for terminal voltage support. Such power factor control is very non-linear, since each rectifier current's magnitude and phase is intimately linked to firing angle and cannot be decoupled.

Generally, to maximise efficiency, the rating of the rectifiers and the load are matched, meaning that changing the proportioning of group dc current by decreasing one rectifier's contribution and increasing the other would overload the latter. If on the other hand, the rectifiers were only partially loaded, altering the current bias within a group would be possible. Additionally, some groups could intentionally be run at rated dc current, with others lightly loaded, or disconnected completely, to increase the multi-group efficiency during periods of partial loading.

In the case of aluminium smelters during commissioning, full current is reached with a minimum number of installed cells, requiring full rated current from all rectifiers in the multi-group, but with low voltage and therefore large firing angles. Conversely, during a smelter restart with a full complement of installed cells, the current profile (similar to that given in Figure 5.4 of Chapter 5) is such that load current could be supplied by some rectifier groups, with others brought online as demand increases.

The goal of such a strategy would be to minimise the number of active MLCRs for a given current order, thus providing the most efficient means of power supply. Two methods of managing this power delivery are explored below.

In the first method, displayed graphically in Figure 6.4, rated current is maintained in all but one active rectifier, with it supplying the balance. In region (a) all the load current is supplied by Group 1 as dc current order is increased. Upon reaching rated current in Group 1, Group 2 is

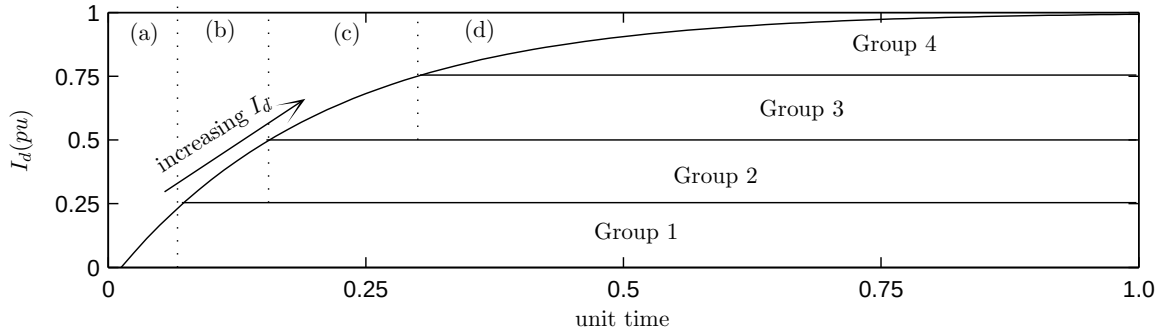


Figure 6.4 Ideal dc current response to minimise losses during increasing current order (In per unit)

enabled (region (b)) and this provides the balance of current, until it too reaches rated current, where Group 3 is enabled and so on. In region (d), rated dc load current is shared equally between the full complement of rectifiers, so as to aggregate the losses.

The second method involves deriving a current order based on the number of active rectifier groups and adding new groups as the current order is increased, spreading the current delivery evenly between active groups. Some additional complexity is caused by the need to coordinate the rectifier-group switch-on based on an overall set point and rectifier rating and also by the controlled disconnection of groups when the current order decreases. To achieve this, a hysteresis band is introduced, so that a new MLCR rectifier is turned on when an increase in order will put the existing rectifier over 100% current rating, and taken off when removing 1 rectifier will result in all remaining rectifiers operating at a safe limit, say 75% of their rating.

The requirements are as follows:

Condition to trigger n+1 rectifier group activation

$$\frac{I_d^*}{rating} > Grps\_active_n \tag{6.17}$$

Condition to trigger n rectifier group deactivation

$$\frac{I_d^*}{((Grps\_active - 1) - deadband^{\dagger}(\%))} \leq Grps\_active_n \tag{6.18}$$

The current order to each of the active groups is

$$I_{d_{grp}}^* = \frac{I_d^*}{(Grps\_active_n)} \tag{6.19}$$

where: I_d^* = Load current order
$I_{d_{grp}}^*$ = I_d group order
Grps_active_n = number of Groups active

rating = rating of rectifier
deadband† = 1 - minimum loading (%)

The methods of operation described above assume that full current is reached at full rated voltage, a condition that is only true if the full dc load is installed and the current order varied, like that which occurs during a restart, as covered in Chapter 5.

6.3.2 Controller Design

The control system block diagram capable of implementing both methods of control is shown in Figure 6.5.

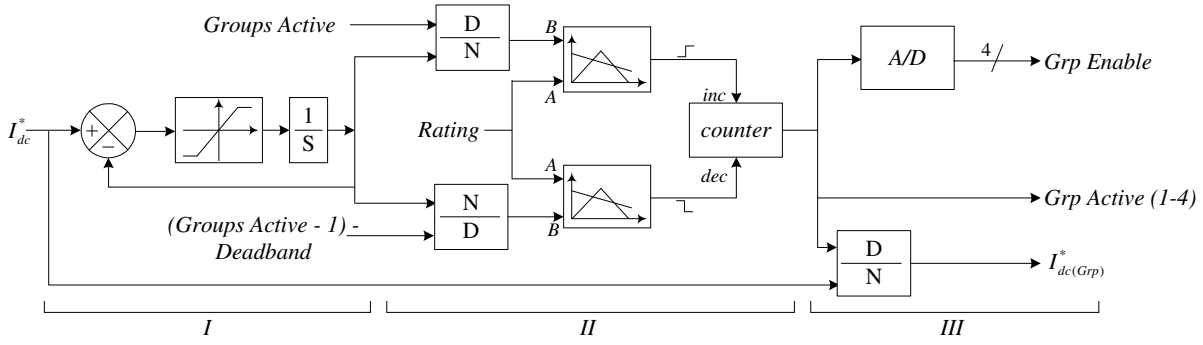


Figure 6.5 Multi-group Rectifier scheduler

Section (I) consists of a hard limit block and integrator which are configured as a simple integral controller through the use of negative feedback. When a change in current order is required, an error signal is generated from the difference between the present current order and the new order. The error magnitude is conditioned by user-defined bounds through the hard limit block and the resulting signal is integrated, again with user defined values. By selecting suitable parameters the overall signal ramp rate can be controlled and the response for small changes is unaffected.

The conditioned current order is fed as the input into part II where the two comparator blocks determine the number of groups to be activated, based on ratings and hysteresis. The upper comparator performs the increment function as in equation 6.17 and the lower performs the decrement function as in equation 6.18. The actual comparison block works as follows; when signal A increases to the point where it exceeds signal B, a pulse is output. In the case of the upper comparator, this corresponds to a counter increase (incrementing the number of groups active by 1), while the lower corresponds to a counter decrease.

Section (III) takes the counter output and provides the group I_d order and raw enable/disable signals to the rectifier groups. It also outputs a status level of how many groups are active.

Another important point is the possible $\frac{dI}{dt}$ at turn off if a rectifier group is deactivated with current still flowing in it, and the resulting negative V_d spike which can be several kV in magnitude. To ensure that abrupt removal of a parallel rectifier does not occur when a reduction in current order is requested, two things must happen. First the zero current order must wait until a 'deactivate' command is given, and second, the thyristors must only be turned off when current in the group falls to zero, thus allowing natural commutation to occur and preventing $\frac{dI}{dt}$ related voltage spikes. The logic required to correctly enable and disable the firing circuits is shown in Figure 6.6.

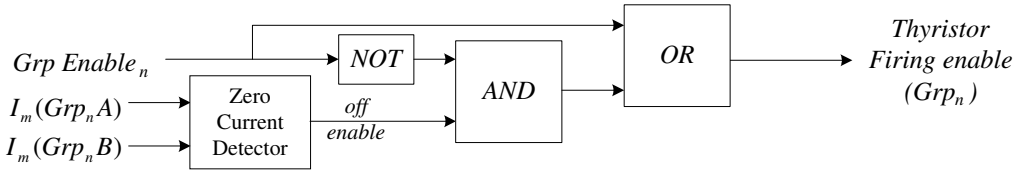


Figure 6.6 Group enabler logic

The current order for each group is derived from simple PID feedback loops, as shown in the block diagram in Figure 6.7. With reference to the figure, the input to the group controller is

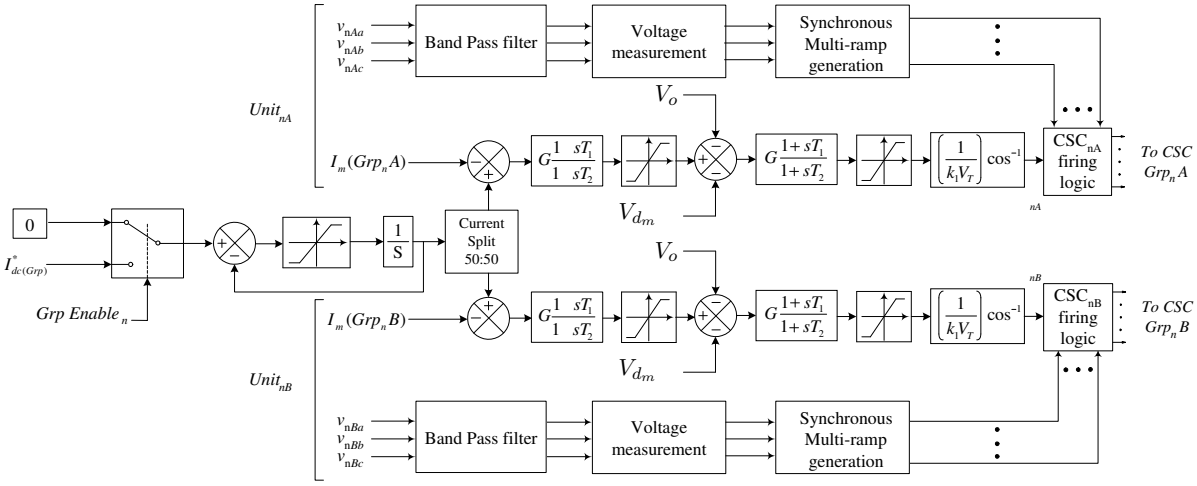


Figure 6.7 Rectifier group control and Firing logic for Group 'n'

rate limited to restrict $\frac{dI^*_{d(grp)}}{dt}$, particularly during the activation of an additional group, using the same order conditioning technique as in Figure 6.5 (I) but with a much faster integration rate. The conditioned signal is split equally between the leading and lagging controllers (upper and lower in Figure 6.7) and becomes the current order for each unit. The error input to the lead-lag compensator (PID) block is determined by the difference between the measured group I_d and current order, whose output is rate limited and then passed as dc voltage order to the voltage controller. A second lead-lag compensator derives the firing angle order, which is scaled by the measured ac terminal voltage.

From there, the firing angles (α_{nA} and α_{nB}) are fed into the Thyristor firing logic, derived from multi-ramp Phase Locked Loops (PLLs); each unit using its filtered ac terminal voltage on the transformer low voltage side as a reference in preference to the common ac bus.

The control block diagrams in Figures 6.5 to 6.7 are also modular to enable virtually any number of groups to be paralleled. The controller gain parameters must be the same for all rectifiers, so that if a change in current order occurs when all rectifiers in the multi-group are active, all will respond at the same rate, thereby ensuring that current sharing between groups is maintained.

6.4 SIMULATED PERFORMANCE OF AN MLCR SMELTER

6.4.1 Test System

The test system of Figure 6.8 consists of 8 identical 48-pulse MLCR rectifiers which are paired into 4 groups, forming a 300 MW smelter dc power supply. A Thevenin source represents the incoming transmission system, with the source voltage (V_s) and source impedance (X_s) specified as 220 kV and 0.17 H respectively. Transformer Tx_1 provides 33 kV to a common ac bus (V_{bus}), which feeds each of the 3-winding star-delta MLCR rectifier transformers.

In the figure, the $_A$ subscript denotes a rectifier with a leading, and $_B$ with a lagging firing angle. Each of the rectifier dc outputs are paralleled through small intergroup reactors ($L_{m1A} - L_{m4B}$) which permit small instantaneous differences in dc voltage. The rectified dc voltage outputs from these groups range from 0 to 1100 Vdc unloaded.

The dc load is represented by a resistance and a small back emf of $1.5m\Omega$ and 420 V respectively, with V_d and I_d representing the load dc voltage and current measurements.

All transformer leakage reactances are specified as 10%, which when combined with X_s provide the system with an SCR of approximately 3.

6.4.2 Dynamic response

The test system is modelled using PSCAD/EMTDC package and a series of step changes is made over an 24 second period to emulate smelter commissioning, on-load maintenance, restart and normal operation, the results of which are presented in Figure 6.9.

The magnitude and timing of the step changes are identical to that of Chapter 5, section 5, so that a direct comparison may be made. A summary of the steps in current order and number of installed cells are given in Table 6.1.

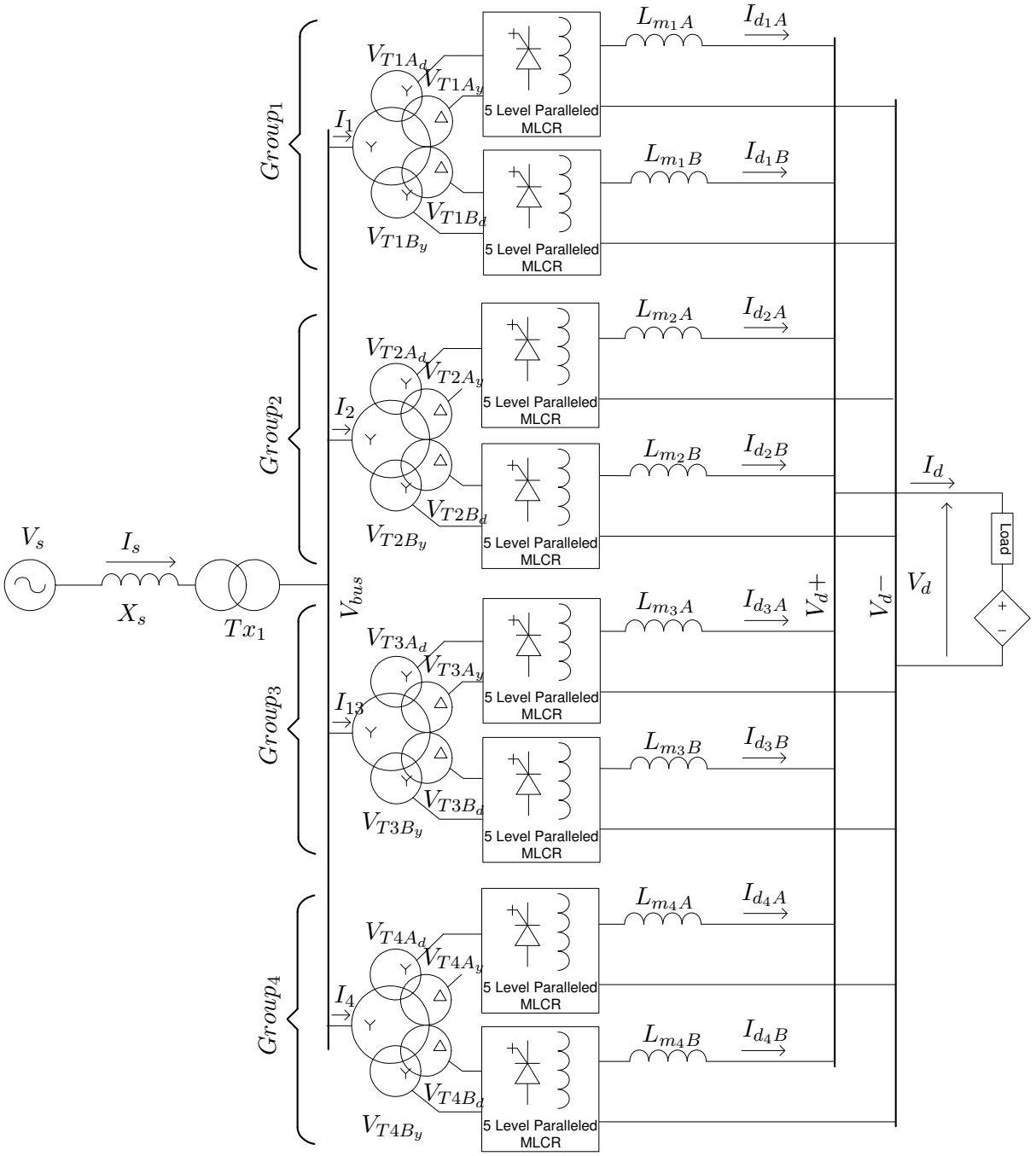


Figure 6.8 Paralleled test system comprised of four 48-pulse reinjection groups

The simulation is started with a current order of 10% to energise all rectifiers, followed by a 100% current order at $t = 1s$. Commissioning of the smelter potlines is initiated at $t = 5s$ where additional cells are connected in stages until 100% are in operation at $t = 7.5s$. The rectifiers are all issued with an equal current command and the measured current in Figure 6.9(c) maintained evenly across all rectifiers (hence the singular trace).

At $t = 12s$ the shut-down command is given, the reduction in total dc current observed in

Table 6.1 Summary of step changes for simulation in Figure 6.9

time(s)	0.15	1	5	5.5	6	6.5	7
$I_{d_{order}}$	25%	100%	100%	100%	100%	100%	100%
Installed cells	14%	14%	28%	43%	57%	71%	86%
time(s)	7.5	9	10	12	15	16.5	18.25
$I_{d_{order}}$	100%	90%	100%	0%	25%	70%	100%
Installed cells	100%	100%	100%	100%	100%	100%	100%

Figure 6.9(b). From $t = 13.25s$ to $t = 14.65s$ a slight difference in dc current response is noticeable between the lagging and leading rectifiers in 6.9(c), with a slightly faster decrease rate from the latter.

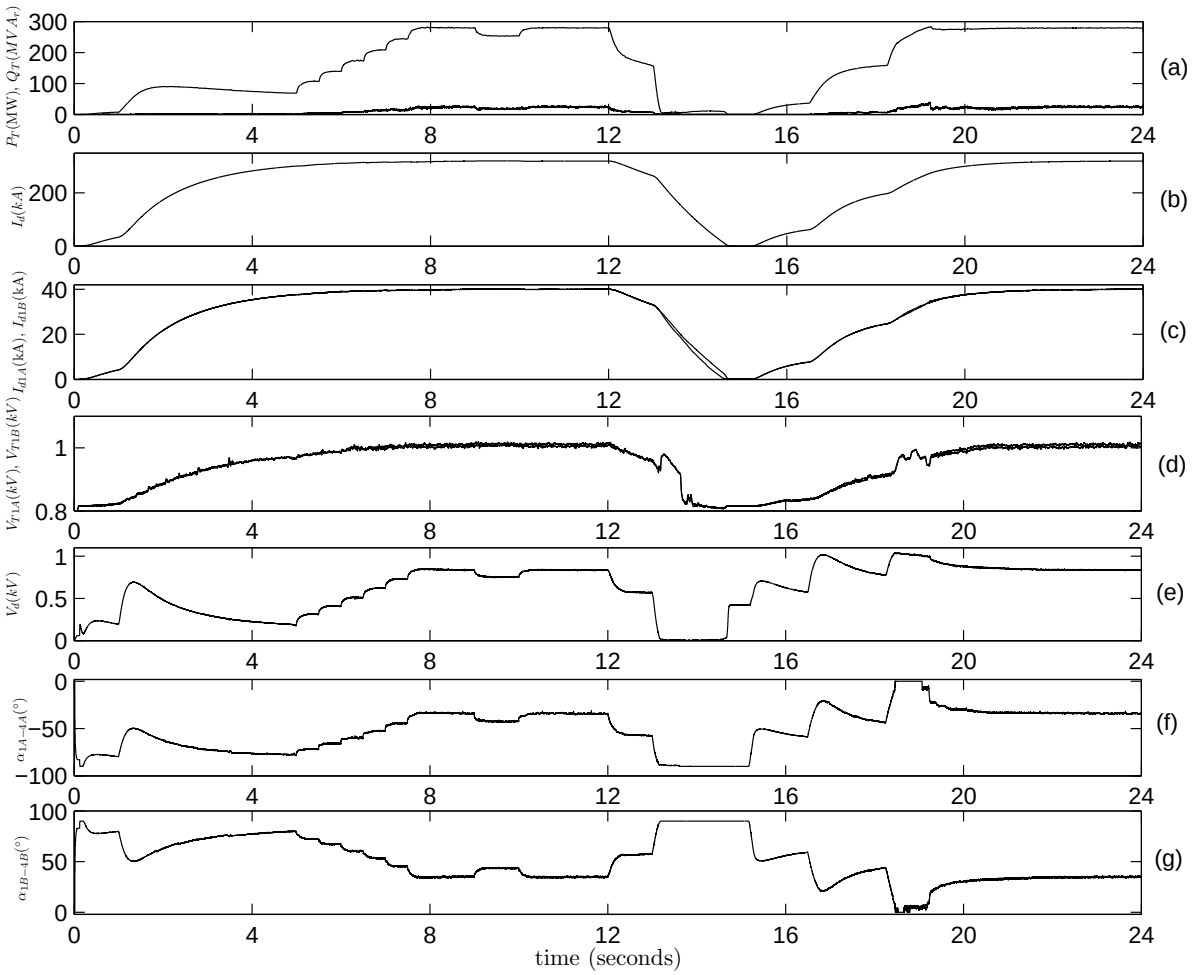


Figure 6.9 Control responses of four MLCR rectifier groups to a series of step changes with (a) total real and reactive power, (b) dc current, (c) group currents, (d) ac terminal voltages, (e) dc voltage, (f) leading firing angles, and (g) lagging firing angles

When a decrease in dc current order is given, each rectifier reduces its absolute firing angle. For the leading rectifiers an immediate consequence of this is a lower ac terminal voltage to that

prior to the decrease command. Conversely, the lagging rectifiers observe an increase in relative terminal voltage.

As a result the lowering terminal voltage of the leading rectifiers reduces the maximum dc voltage proportionally, assisting in current decrease, while increased terminal voltage hinders the lagging type.

From the control diagram of Figure 6.7, the phenomenon is partly compensated in the voltage controllers by terminal voltage scaling prior to firing angle output, but since the terminal voltage is a calculation performed over time, and averaged to minimise noise, it exhibits a slight delay, which prevents ideal compensation. Since minimal real power is drawn from the power system during this period, the effect on the network is minimal.

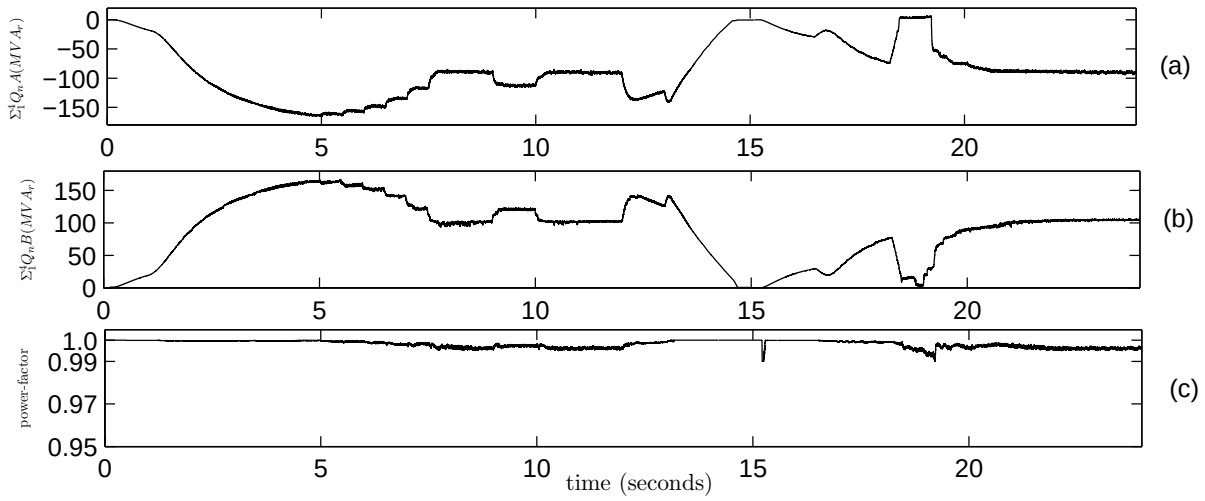


Figure 6.10 Reactive power contributions and overall smelter power-factor, with (a) total reactive power generation, (b) reactive power absorption, and (c) power-factor as seen from transmission system

Smelter restart begins at $t = 15s$ where a 64 kA (20%) current order is given, followed by a 225 kA (70%) order at 16.25 s, and finally a 320 kA (100%) current order at 18.25 s, with normal operation recommencing at approximately 19.2 seconds.

The active and reactive power responses on the high voltage side of the supply transformer (T_{x1}) are given in Figure 6.9(a). The leading and lagging reactive power contributions of each of the rectifiers are shown in Figures 6.10(a) and (b) respectively. High power-factor operation is seen to be maintained (Figure 6.10(c)), with an average of 0.997 (4.45° lagging) observed during normal operation and dropping briefly to 0.99 (8.1° lagging) during restart (at about t=19.0 s); this is due to the reactive power demands of all transformers when the rectifiers operate at zero firing angle.

Once again, the timescale used in this simulation is indicative only, as the cell commissioning

period alone could take up to 6 months to complete. Similarly a restart would take much longer in practice, a period of 30-60 minutes typical.

6.4.3 Waveform Quality

The supply current, leading and lagging current waveforms of the multi-group MLCR rectifier are given in Figure 6.11. The waveform snapshot is taken at rated current, and the multi-level waveform steps are clearly evident for the leading rectifier in Figure 6.11(b) and lagging rectifier in 6.11(c).

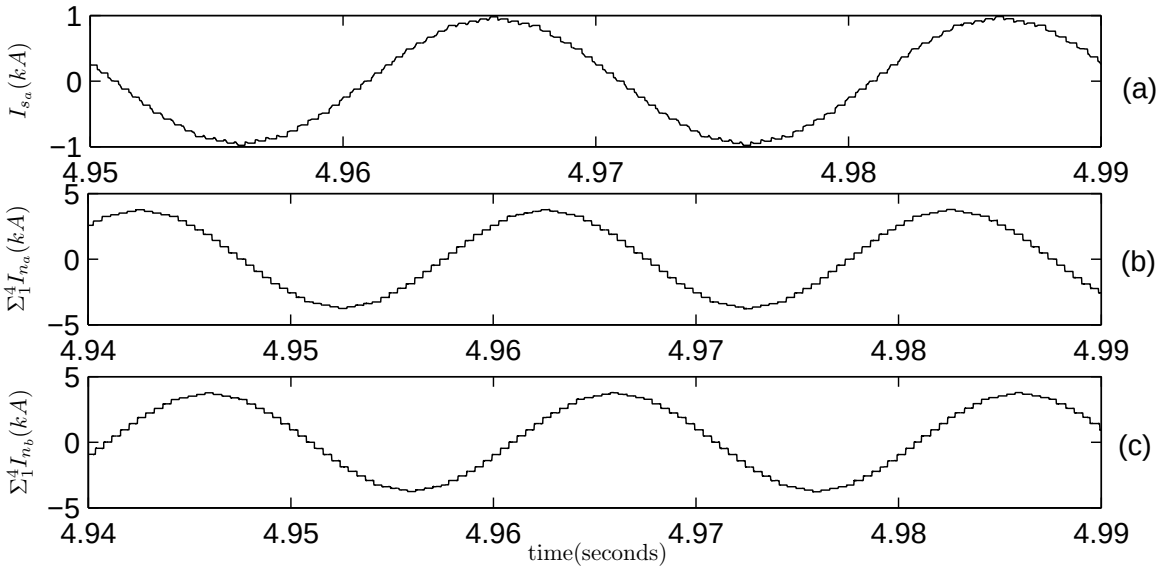


Figure 6.11 AC currents for the multi-group MLCR rectifier, with (a) the combined supply current, (b) leading rectifier current, and (c) lagging rectifier current

The harmonic components of Figure 6.11(a) are analysed and the results shown in Figure 6.11. The predominant 47^{th},49^{th} harmonic has a magnitude of 2%, with the 11^{th}, 13^{th} at 0.9%, 45^{th}, 97^{th} at 0.57% and 143^{th}, 145^{th} at 0.42%, which combine for a total harmonic distortion (THD) of 3.01%.

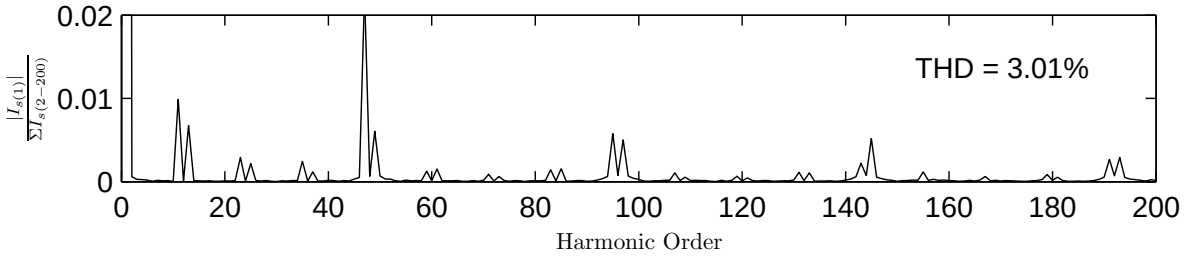


Figure 6.12 Multi-group MLCR ac supply current (I_a) harmonic performance for the first 200 harmonic orders

6.4.4 MLCR Multi-group reactive power controllability

Given that the MLCR rectifiers are capable of controlling their dc currents directly, several options exist to alter the reactive power characteristics of the multi-group, to potentially improve operating efficiency, reduce restart time or to provide additional voltage support to the power system. With the reactive power contribution of rectifier $_n$ given by

$$Q_n = \sqrt{3} k_1 V_{T_n} I_{d_n} \sin(\alpha_n) \tag{6.20}$$

adjusting the rectifier's terminal voltage (V_{T_n}), dc current (I_{d_n}), conversion constant (k_1), and firing angle (α_n) each have a direct effect on the reactive power characteristics of the rectifier. While changing the terminal voltage and conversion constant require hardware changes, the dc current and firing angle may be manipulated purely by modifying the control method, and thus several potential control variations arise to improve on the multi-group reactive power characteristics. They are:

- The number of rectifiers active may be changed if the dc current demand permits (i.e. if the dc side is partially loaded)
- The balance of current within a group may be biased to either the leading or lagging rectifier (within a small amount if fully loaded) to make the group a net generator of reactive power
- The lead/lag ac current balance across the entire multi-group may be altered
- Reversal of the firing angle polarity of one or more of the rectifiers in the multi-group to alter reactive power generation

Performance of each of the altered configurations is compared to the base case as given in Figure 6.9 and is shown as a dotted reference trace on each of the Figures 6.13 to 6.18. The measure of performance improvement is made by determining operating efficiency in each case; by comparing reactive power demands, and ac supply current magnitude. Incidentally, multi-group efficiency is calculated as

$$\text{efficiency}(\varepsilon) = \frac{P_T}{V_d \times I_d}(\%) \tag{6.21}$$

for each situation, with P_T representing the measured ac power at the HV terminal and $V_d I_d$ the measured dc power.

The following test cases are performed on the same system used in Section 6.4.2 (with and SCR of 3), and may not be as applicable in a stronger system, where terminal voltage variation with changing reactive power demands is less.

Demand based dc current staggering

The first configuration is made in accordance with the control theory in figures 6.5 to 6.7 in section 6.3.2, to analyse the performance of enabling the rectifier groups on demand. The results of this simulation over a seven second period are given in Figure 6.13.

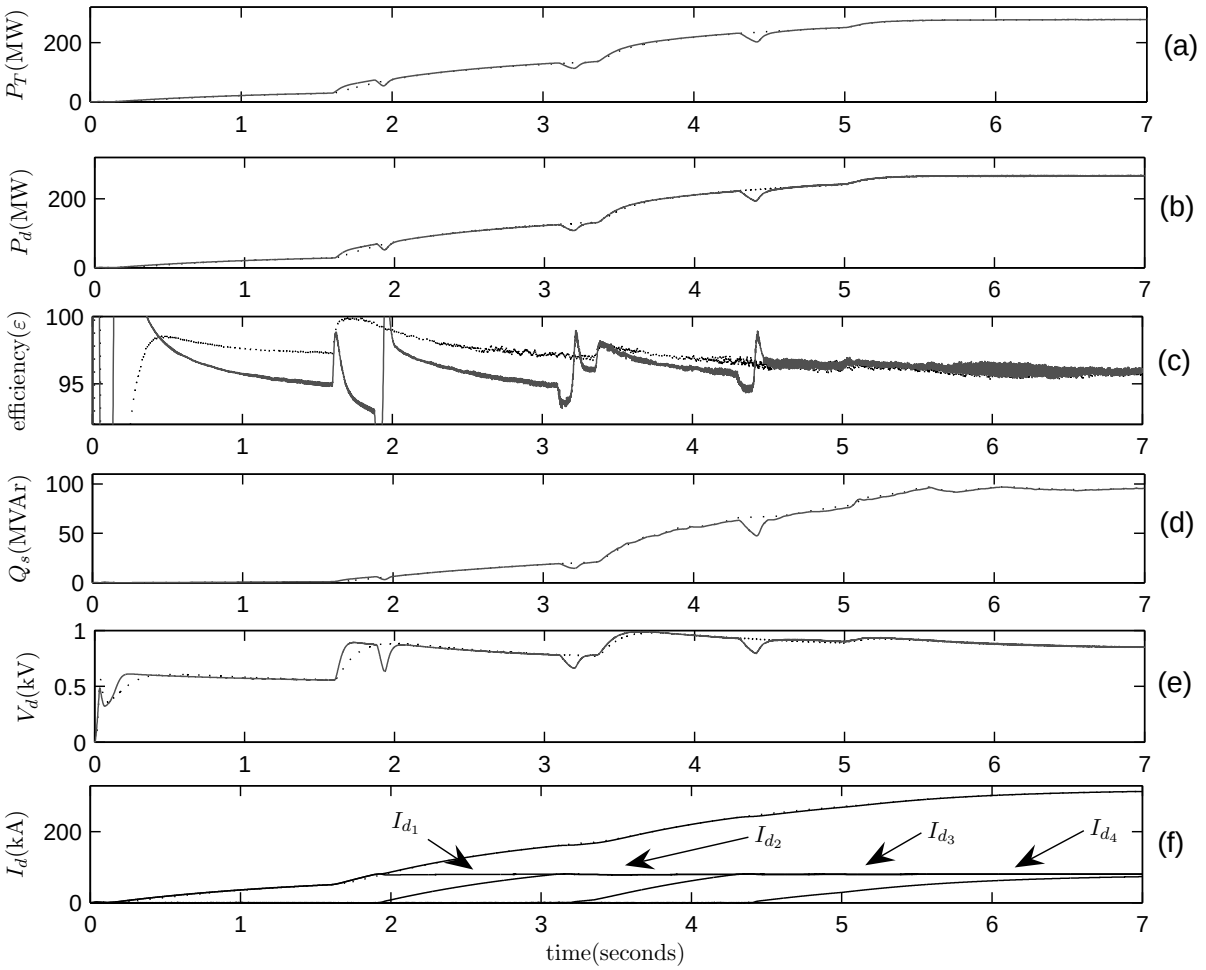


Figure 6.13 Simulated performance of a multi-group Rectifier with staggered current share

The first rectifier pair are activated and supply all dc current until demand increases above rated (80 kA), where another pair is activated at t =1.9, 3.1 and 4.3s. Graph 6.13(a) is the input power, graph (c) the efficiency, graph (d) the reactive power as observed from the source, (e) the dc load voltage, and in this case, (f) the dc current contributions of each of the rectifier pairs and total dc current.

From graph (a) the input power change is minimal, aside from small perturbations as each new group is activated, as evident in all traces at 1.75, 3.2, and 4.4 s. Comparing the traces of graph (c), this configuration is actually less efficient in transitioning from zero to full load current as

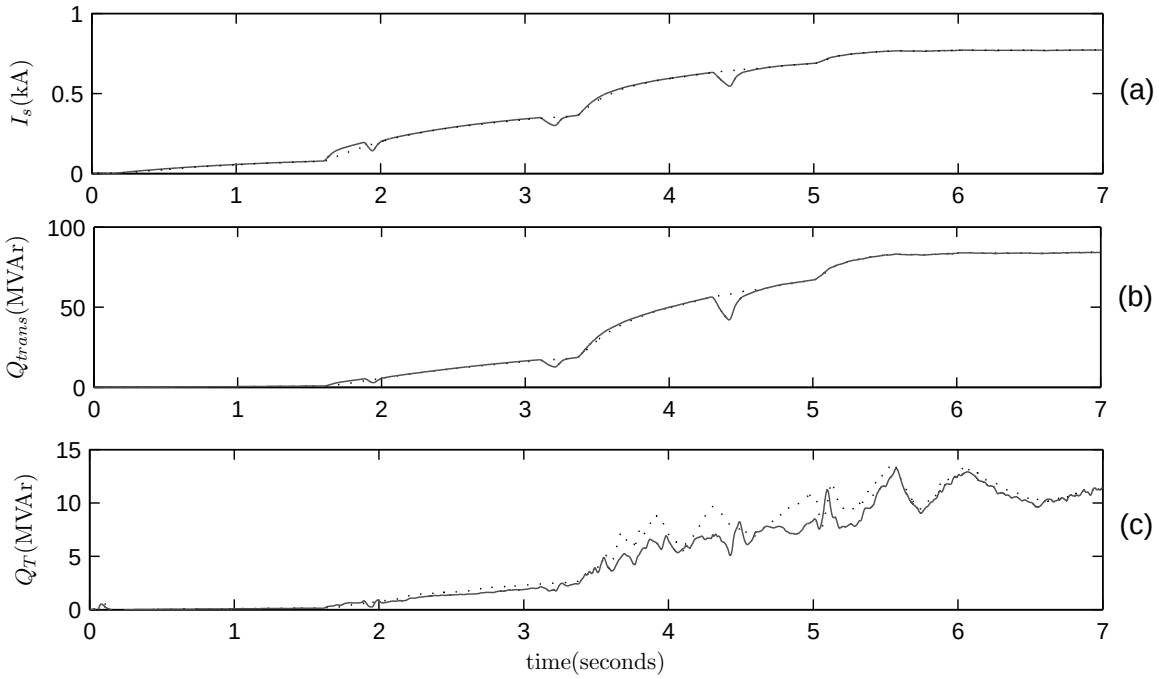


Figure 6.14 Multi-group reactive power performance with staggered current share

compared to the dotted reference trace. The lower efficiency is due to the amount of time that each new rectifier pair must have its firing angle at 0° (i.e. maximum dc voltage) to establish current flow. As the rate of current increase in a new group depends on the difference between load voltage and maximum dc voltage, the current rise takes longer as load voltage is raised. Previously with all rectifiers working in unison, that is, the same dc current, there were few excursions to 0° firing angle during an increase in current, as all rectifiers worked together to increase a common dc voltage, so their individual increase rates were less and thus required less dc voltage for a given current rise.

The supply current in 6.14(a) and the reactive power demands in 6.13(d) and 6.14(c) show negligible improvement over the whole simulation period.

DC current bias within the multi-group

Altering the balance of dc current spread between leading and lagging rectifiers has the potential to change the amount of reactive power generated or absorbed by the multi-group. The effects of altering the current share between a leading and lagging rectifier are the same whether a pair of rectifiers or a whole multi-group have their current split altered. For this reason the simulation is carried out with adjustment made across the whole multi-group.

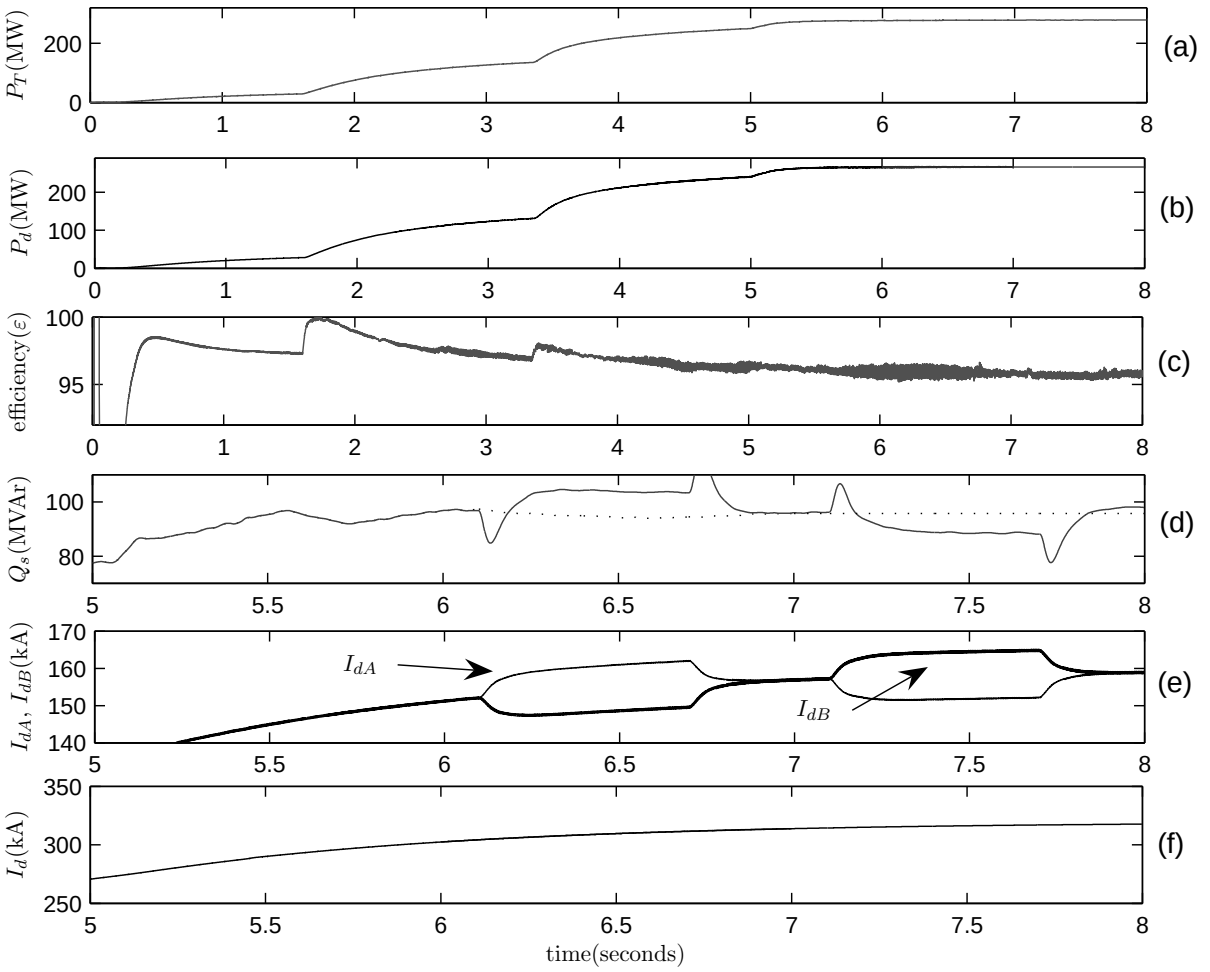


Figure 6.15 Multi-group reactive power performance with dc current biased to the leading and lagging rectifiers as compared to the base case (dotted trace in (d))

The multi-group simulation in Figure 6.15 is initialised as in the base case and allowed to stabilise at full dc current, which occurs at approximately $t = 6s$. At $t = 6.1s$ the dc current order of the leading group is increased by 4kA (corresponding to 1 kA per 48-pulse MLCR rectifier) and the lagging group reduced by the same amount. The immediate effect as seen in Figure 6.15(d) is an increase in reactive power absorption by the multi-group, up 10 MVAr from 94 MVAr to 104 MVAr. At $t = 6.7s$ the dc current bias is returned to the original even split. At $t = 7.0s$, the dc current of the lagging rectifiers are increased, with an immediate reduction in reactive power absorption in (d) from 94 MVAr of the base case, to 88MVAr. At $t = 7.6s$ the 50:50 dc current split is restored. The reactive power and supply current traces of Figure 6.16 exhibit a similar response as expected, with the reactive power absorbed by the rectifier and supply transformers in (c) reduced significantly. The ac and dc powers of Figure 6.15(a) and (b) are unchanged as are the efficiency and dc current in (c) and (e) respectively.

The reactive power absorbed by the multi-group in this example under the operating conditions

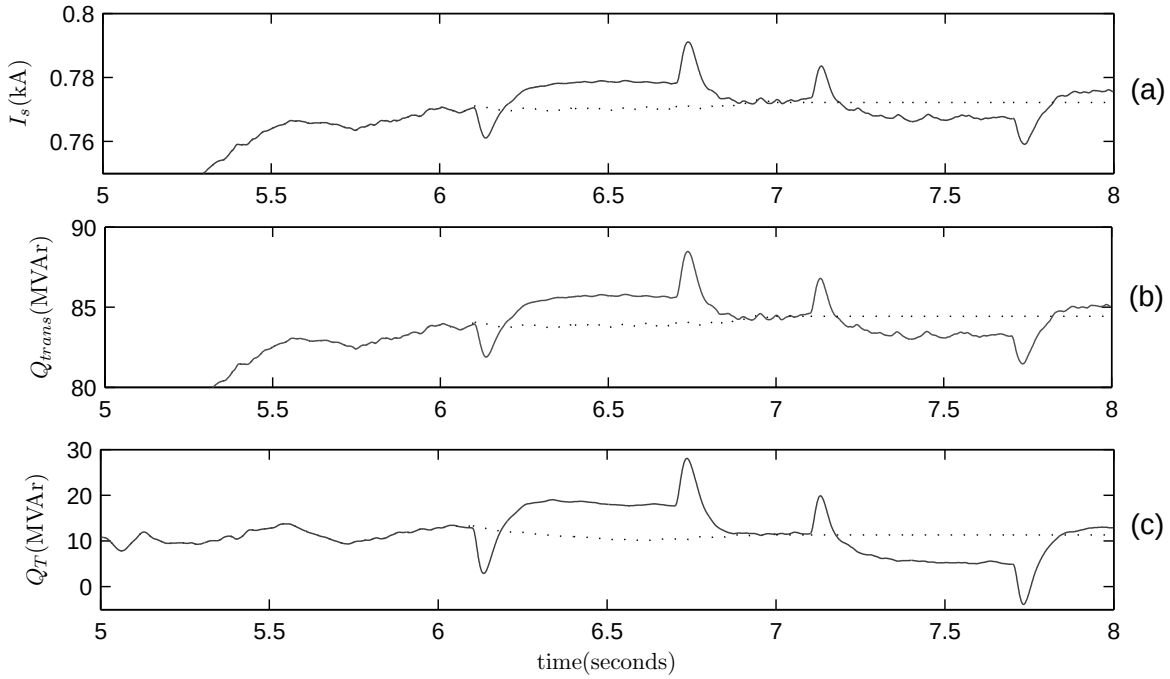


Figure 6.16 Multi-group reactive power performance with dc current biased to the leading and lagging rectifiers as compared to base case

given in section 6.4.2 is thus affected more by changes in firing angle than by current order, or with reference to equation (6.20)

$$\frac{dQ_n}{d\alpha_n} > \frac{dQ_n}{dI_{d_n}}$$

as the sensitivity of the multi-group reactive power to a change in firing angle is greater than that of an increased dc current.

The reduced reactive power demand does come at the expense of an increased dc current rating in the lagging group, but in this case a 2.5% increase in current reduces the reactive power absorption by 9%, which may be an acceptable design consideration.

Obviously under different load conditions, or when connected to a transmission system of differing impedance, the firing angles for maximum power transfer will differ and this relationship and method of control may no longer be possible.

Firing angle polarity reversal within the group

The multi-group rectifiers modelled in these simulations are fed from a relatively weak transmission system and as a result, the optimum firing angles for maximum power delivery are, for the high power-factor multi-group, -35° for the leading and 34° for the lagging groups, under

steady-state conditions and when current is balanced. In the base case 91MVAr is drawn from the ideal source through the transmission system.

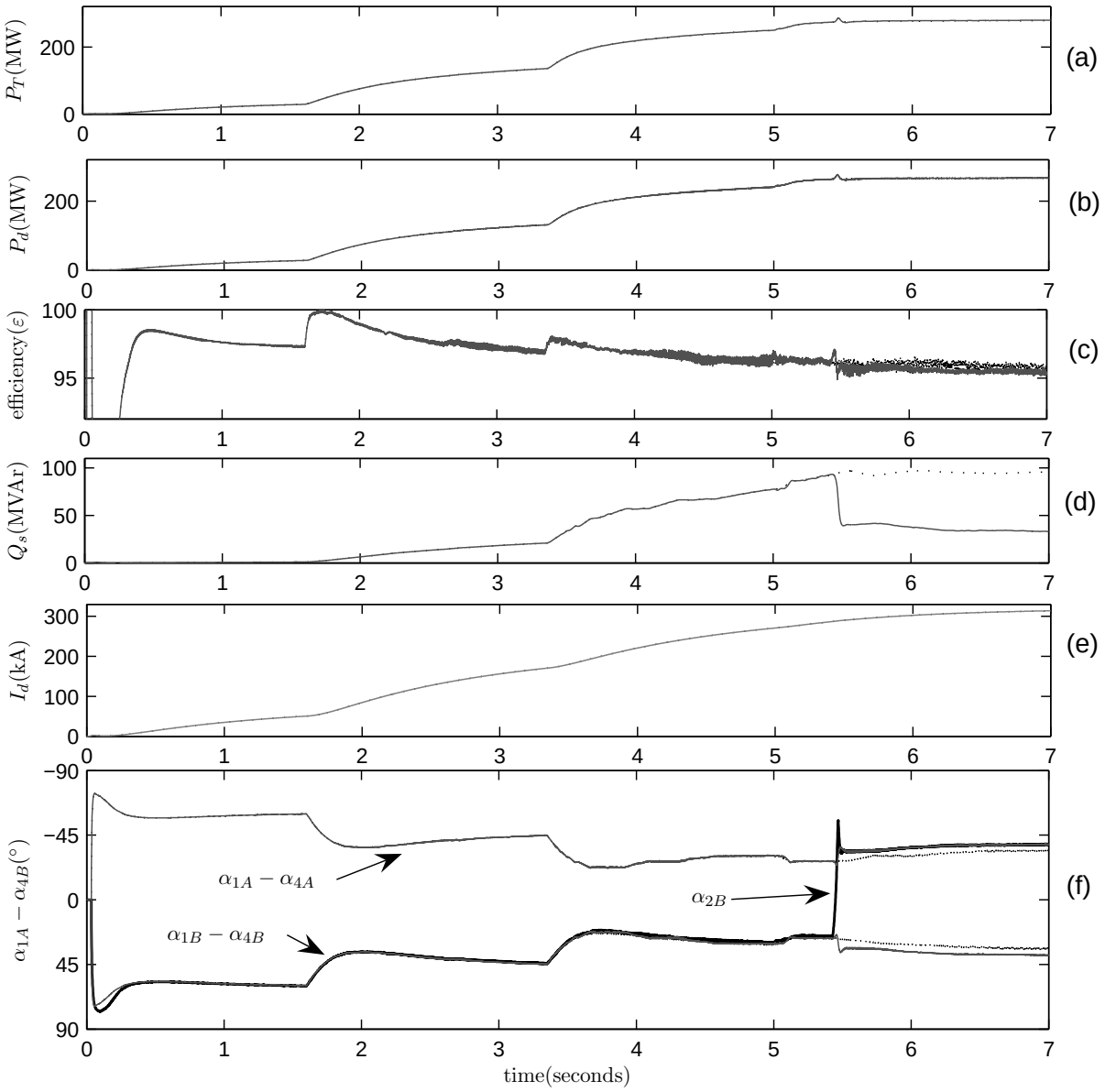


Figure 6.17 Multi-group performance with controlled polarity reversal of firing angle α_{2B} as compared to base case

At full load, the reactive power circulating in each of the MLCR groups is approximately 20 MVAr generated by the leading rectifier and 20 MVAr absorbed by the lagging. If one lagging rectifier were to have its firing angle advanced so that it was leading, but with the same dc voltage, the dc contribution would be the same but the reactive power generated by the group would be 40 MVAr. This control opportunity is exploited in Figure 6.17(f) at $t = 5.5s$, with the polarity of firing angle α_{2B} changed on-load, taking advantage of the long dc current time

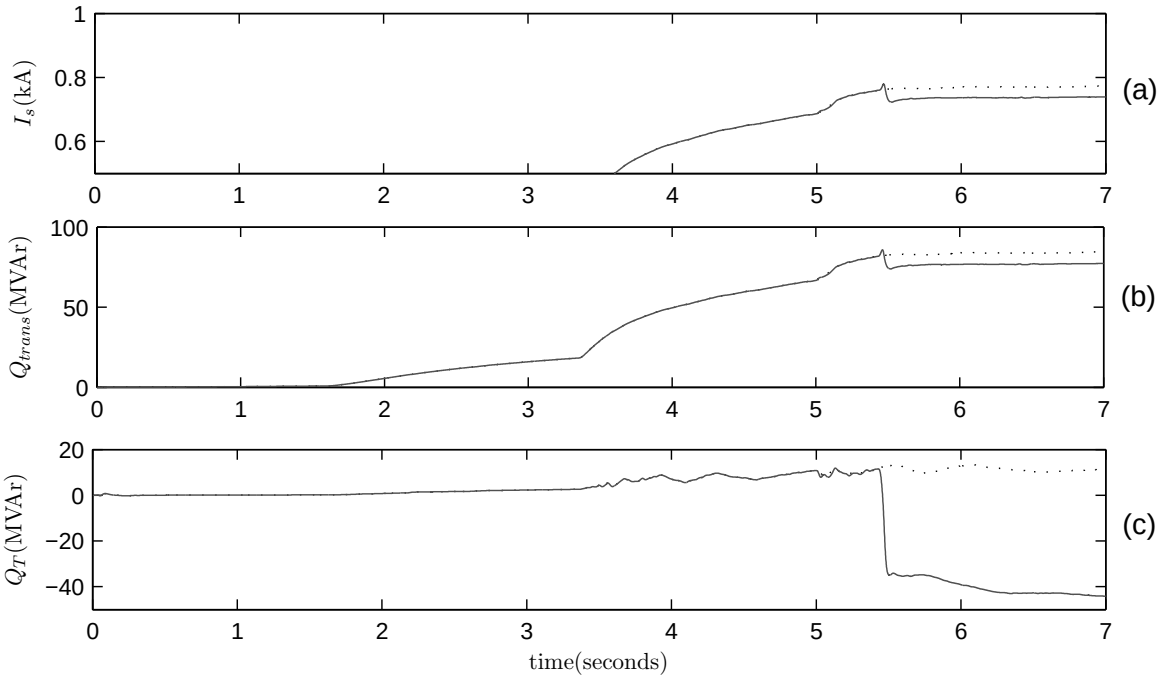


Figure 6.18 Multi-group reactive power performance with controlled polarity reversal of firing angle α_{2B} as compared to base case

constant as compared to the reactive power polarity change time. Consequently, as shown in Figure 6.17(d), this increased reactive power contribution from the multi-group partially corrects for the reactive power absorbed by the transmission system (Figure 6.18(b)), reducing the complex voltage drop and the apparent power from the source, thus reducing the supply current, as seen in Figure 6.18(a), from 0.771 kA to 0.737 kA, and the associated transmission losses. The result of this is the possibility of increased maximum power transfer, increased transmission efficiency, and a further increase in firing angle for a given dc load.

Consideration must be made for the other rectifiers supplying dc current, as advancing one rectifier's firing angle through zero will increase its dc voltage to maximum, potentially overloading that rectifier and reducing the apportioned current to the remaining rectifiers. If the time taken to change from lagging to leading firing angle is much shorter than the dc current time constant, the effect on the dc current share will be negligible, but the real power of the advancing group will increase momentarily. In Figure 6.17(a) and (b) there is a small increase in both ac and dc powers of approximately 5%, but its duration is only 50 ms. Likewise, there is a small difference in efficiency, but that settles quickly back to 96.1%.

Depending on the dc operating conditions, the ratio of leading to lagging firing angles could be set before the multi-group rectifiers are started, or polarity could be changed under load as reactive power demands of the connected power system change.

With respect to aluminium smelter operation, this control method may not be suitable during commissioning, with the low dc voltage(and thus large firing angles) at rated current would mean a large imbalance in reactive power circulation, and potentially an undesirably high terminal voltage. In this case the firing angle polarity would need to be switched under load at near full rated dc voltage.

6.5 CONCLUSIONS

A high power two-quadrant parallel-MLCR based high current rectifier has been developed and extensively tested using PSCAD/EMTDC with reference to a 300 MW smelter.

Two 5-level (48-pulse equivalent) MLCR rectifiers with firing angles of opposing polarities are parallel connected on both the ac and dc sides, and with a common dc voltage, form a high current, high power-factor group. Since the groups are modular, several are parallel connected to achieve the high dc current required by the smelter load.

In contrast to the 12-pulse rectifiers in Chapter 5, each MLCR rectifier has high pulse operation without costly phase-shifting transformers, and can therefore directly control dc current without affecting ac current waveform quality. By increasing dc current in either the leading or lagging rectifiers, additional reactive power control is possible, with reactive power generation used to support terminal voltage and reduce transmission losses.

As well as improving harmonic performance, the multi-level switching reduces switch stresses as compared to the basic 12-pulse bridges in Chapter 5. The MLCR rectifier's main bridge zero current switching also removes thyristor commutation angle, although it does require self-commutating switches of full rectifier current rating in the reinjection circuit.

Both the MLCR and 12-pulse (phase-shifted) self-commutating switches must be rated at full rectifier current. Self-commutated thyristors have about double the on-state voltage drop of their line-commutated counterparts, so the on-state losses of the MLCR (two thyristor and one IGCT) are about the same as a 12-pulse self commutated bridge rectifier (two IGCTs). For the added control flexibility of the MLCR, the extra self-commutating switch is easily justified.

In summary, the two-quadrant parallel-MLCR rectifier possesses more control flexibility and simpler transformer connection than a phase-shifted thyristor based equivalent, and thus presents an appealing alternative in high current high power-factor current-sourced conversion.

Chapter 7

HYBRID THYRISTOR-MLCR HIGH CURRENT RECTIFIER

7.1 INTRODUCTION

High power thyristor based rectifiers are becoming viable in extremely high current, dc applications (such as smelters), gradually replacing the OLTC and diode rectifiers for increased active power controllability.

Their main drawback in high-power high current rectification is the absorption of reactive power with increased firing angle delay, the effects of which must be compensated, or implicitly controlled to correct power-factor as covered in Chapters 5 and 6.

To correct poor power-factor and preserve waveform quality at high power, high-pulse reactive power compensation is necessary, using either voltage source or current source based Statcoms. Preference is generally given to VSC based schemes [55, 56, 57], with the dc side capacitor providing superior energy storage efficiency to the CSC's large and lossy dc side inductor.

However, CSC based reactive power compensation possesses advantages over VSCs for control of dc voltage and current. In a high current application the CSC's dc inductor may be eliminated, if its dc side is parallel connected to the high current dc load bus, and the CSC Statcom's rectified current instead smoothed by the load impedance. This enables the Statcom to supply some active power to the dc load, but with a large leading firing angle (by way of its lower transformer winding ratio) to efficiently generate the necessary reactive power to correct power-factor to unity.

This chapter describes a hybrid rectifier configuration that uses efficient Thyristor based rectifiers in the main conduction path and a high-pulse MLCR in parallel to provide a small real power contribution but the balance of the reactive power generation.

7.2 THE CONTROL CONCEPT

Figure 7.1 presents a block diagram of the hybrid configuration. For simplicity several phase-shifted thyristor rectifiers are shown as one power block so their applicability to any number of pulses can be retained. The relative sizes of the components are used to illustrate that the majority of power transfer is through the thyristor bridges.

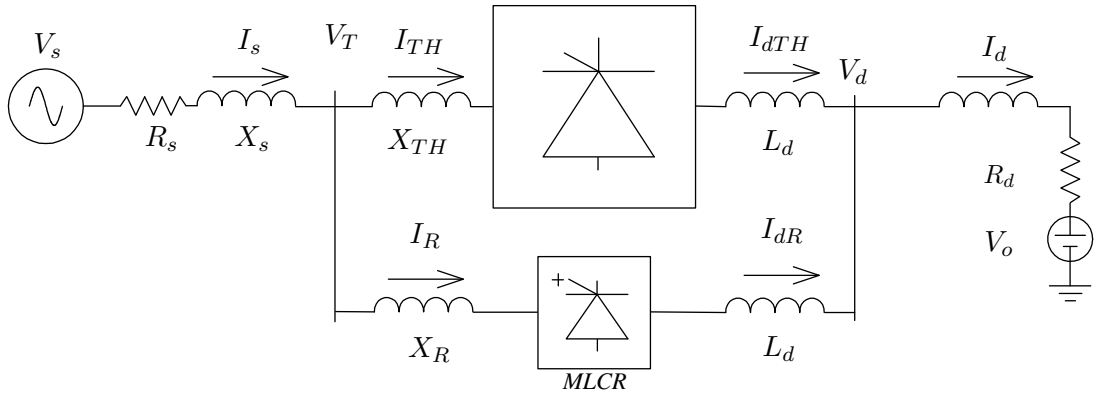


Figure 7.1 Simple block diagram of a hybrid Thyristor MLCR based smelter power supply

The rectifiers are supplied from an ac system represented by a Thevenin equivalent circuit consisting of source voltage V_s and series impedance (X_s and R_s), which in turn feeds a common ac bus with voltage V_T. The transformer leakage reactances are signified by X_{th} and X_R for the thyristor and MLCR branches respectively. The bridges are also paralleled on the dc side, with small intergroup reactors (represented by L_d) included to allow for small instantaneous mismatches in dc voltage.

An idealised phasor diagram of the configuration is shown in Figure 7.2.

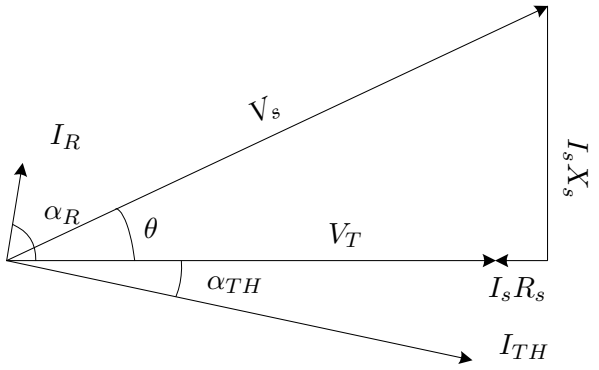


Figure 7.2 Phasor diagram for a hybrid Thyristor MLCR based smelter power supply

The source and terminal voltages, V_s and V_T respectively, are separated by the phase-shift created by the supply current (I_s) and thevenin impedance (X_s and R_s). Thyristor firing angle

(α_{TH}) and ac current (I_{TH}) are referenced to the terminal voltage (V_T), as are the MLCR firing angle and ac current are represented by α_R and I_R respectively. The magnitudes of each of the ac currents provide the same amount of reactive power, but their real power components differ greatly.

To enable the large reactive power correction needed for high power factor operation whilst maintaining high efficiency, a reduced transformer ratio is used on the MLCR bridge. Increasing the secondary output voltage of the MLCR rectifier permits full dc load voltage to be developed at a large firing angle, and thus large reactive power compensation for a small real power output. This topology exploits the relationship between Q_R (MLCR Reactive power) and α_R (MLCR firing angle) in the following equation:

$$Q_R = \sqrt{3} k_R I_{dR} V_T \sin(\alpha_R) \tag{7.1}$$

For a specified reactive power level (Q_R) and rated dc current (I_{d_R}), increasing constant k_R (the MLCR transformer turns ratio) must be coupled with a decrease in $\sin(\alpha_R)$. Thus with a suitable k_R and α_R near $-90°$, a small change in α_R will yield a large change in I_{d_R}, and therefore a large change in Q_R. Put simply, $\frac{dQ_R}{d\alpha_R}$ near $-90°$ is small and negative, whereas $\frac{dQ_R}{dI_{d_R}}$ is large and positive by comparison.

In a practical situation, the reactive power compensation level would be known or specified, as would the dc current rating of the MLCR switches and nominal dc load voltage. Considering the firing angle bounds of between $-90 \leq \alpha_R \leq -80°$ where $\cos(\alpha_R)$ is almost linear (regression residuals are all positive with a maximum error of 0.00034) minimum k_R may be calculated as follows:

$$k_R = \frac{Q_{R_{specified}}}{\sqrt{3} I_{R_rated} V_T \sin(\alpha_{R_{max}})} \tag{7.2}$$

This enables predominantly reactive power generation rather than real power and keeps MLCR switch current ratings small, but with a corresponding increase in voltage rating. Given the higher voltage rating and large reactive power demands, the MLCR transformer must be sized accordingly. With the MLCR, maximum dc output voltage will be k_R times that of the thyristor group and the voltage ratings of the MLCR switching components must be increased by the same level.

The ac side function of the MLCR rectifier is similar to conventional reactive power compensation with SVCs or statcoms, in that it draws controlled leading current to maintain high power factor. However, SVCs and statcoms must be rated for the maximum reactive power required, which is only required during starting conditions, and does not contribute to smelter active power.

Conversely, the MLCR rectifier of the hybrid system can provide practically its full dc current rating as active power under normal operating conditions when relatively little reactive power is required.

7.2.1 Circuit equations

In order to control the phase-shifted thyristor and MLCR rectifiers as a single system, the relationships between the real and reactive powers, terminal voltage and dc operating state must be defined.

The real and reactive powers are related to the common terminal ac voltage (V_T) using the orthogonal D-Q transform.

The transform identity matrix $\mathbf{M}$ is defined as:

$$\mathbf{M} = (\mathbf{M}^{-1})^T = \sqrt{\frac{2}{3}} \begin{bmatrix} \sin(\omega t) & \sin(\omega t - 120^\circ) & \sin(\omega t + 120^\circ) \\ \cos(\omega t) & \cos(\omega t - 120^\circ) & \cos(\omega t + 120^\circ) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \tag{7.3}$$

If the 3-phase system is balanced then:

$$\mathbf{I}_s = \sqrt{2} I_s \begin{bmatrix} \sin(\omega t + \phi_1) & \sin(\omega t + \phi_1 - 120^\circ) & \sin(\omega t + \phi_1 + 120^\circ) \end{bmatrix}^T \tag{7.4}$$

$$\mathbf{V}_s = \sqrt{2} V_s \begin{bmatrix} \sin(\omega t + \phi_s) & \sin(\omega t + \phi_s - 120^\circ) & \sin(\omega t + \phi_s + 120^\circ) \end{bmatrix}^T \tag{7.5}$$

Which when transformed become:

$$\mathbf{I}_{s_{dq}} = \mathbf{M}\mathbf{I}_s = \sqrt{3} I_s \begin{bmatrix} \cos(\phi_1) & \sin(\phi_1) & 0 \end{bmatrix}^T = \begin{bmatrix} I_{s_d} & I_{s_q} & 0 \end{bmatrix}^T \tag{7.6}$$

$$\mathbf{V}_{s_{dq}} = \mathbf{M}\mathbf{V}_s = \sqrt{3} V_s \begin{bmatrix} \cos(\phi_s) & \sin(\phi_s) & 0 \end{bmatrix}^T = \begin{bmatrix} V_{s_d} & V_{s_q} & 0 \end{bmatrix}^T \tag{7.7}$$

To simplify the notation, matrix $\mathbf{N}$ is defined as:

$$\mathbf{N} = \begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix}$$

Using the D-Q reference frame the terminal real power (P_T) is calculated as:

$$P_T = \mathbf{V}^{\mathbf{T}}_{\mathbf{T_{dq}}} \mathbf{I}_{\mathbf{s_{dq}}} = P_s - P_L = \mathbf{V}^{\mathbf{T}}_{\mathbf{s_{dq}}} \mathbf{I}_{\mathbf{s_{dq}}} - R_s \mathbf{I}^{\mathbf{T}}_{\mathbf{s_{dq}}} \mathbf{I}_{\mathbf{s_{dq}}} \tag{7.8}$$

and reactive power as:

$$Q_T = \mathbf{V}^{\mathbf{T}}_{\mathbf{T_{dq}}}\mathbf{N}\mathbf{I}_{\mathbf{s_{dq}}} = Q_s - Q_L = \mathbf{V}^{\mathbf{T}}_{\mathbf{s_{dq}}}\mathbf{N}\mathbf{I}_{\mathbf{s_{dq}}} - \omega L_s \mathbf{I}^{\mathbf{T}}_{\mathbf{s_{dq}}}\mathbf{I}_{\mathbf{s_{dq}}} \tag{7.9}$$

where P_L and Q_L are the real and reactive power transmission losses respectively.

As P_T and Q_T are scalars they can be added.

$$\mathbf{I}^{\mathbf{T}}_{\mathbf{s_{dq}}}\mathbf{V}_{\mathbf{T_{dq}}} = \mathbf{I}^{\mathbf{T}}_{\mathbf{s_{dq}}}\mathbf{V}_{\mathbf{s_{dq}}} - R_s\mathbf{I}^{\mathbf{T}}_{\mathbf{s_{dq}}}\mathbf{I}_{\mathbf{s_{dq}}} \tag{7.10}$$

$$\mathbf{I}^{\mathbf{T}}_{\mathbf{s_{dq}}}\mathbf{N}\mathbf{V}_{\mathbf{T_{dq}}} = \mathbf{I}^{\mathbf{T}}_{\mathbf{s_{dq}}}\mathbf{N}\mathbf{V}_{\mathbf{s_{dq}}} - \omega L_s\mathbf{I}^{\mathbf{T}}_{\mathbf{s_{dq}}}\mathbf{I}_{\mathbf{s_{dq}}} \tag{7.11}$$

which combined allows the terminal voltage to be expressed as:

$$\mathbf{V}_{\mathbf{T_{dq}}} = \mathbf{V}_{\mathbf{s_{dq}}} - R_s\mathbf{I}_{\mathbf{s_{dq}}} - \omega L_s\mathbf{N}\mathbf{I}_{\mathbf{s_{dq}}} \tag{7.12}$$

The RMS terminal voltage is then calculated by

$$\begin{aligned} V_{T_{rms}} = \quad & \mathbf{V}^{\mathbf{T}}_{\mathbf{T_{dq}}}\mathbf{V}_{\mathbf{T_{dq}}} = \mathbf{V}^{\mathbf{T}}_{\mathbf{T_{dq}}}\mathbf{V}_{\mathbf{s_{dq}}} - R_s\mathbf{V}^{\mathbf{T}}_{\mathbf{T_{dq}}}\mathbf{I}_{\mathbf{s_{dq}}} - \omega L_s\mathbf{N}\mathbf{V}^{\mathbf{T}}_{\mathbf{T_{dq}}}\mathbf{I}_{\mathbf{s_{dq}}} \\ = \quad & \mathbf{V}^{\mathbf{T}}_{\mathbf{T_{dq}}}\mathbf{V}_{\mathbf{s_{dq}}} - R_sP_T - \omega L_sQ_T \end{aligned} \tag{7.13}$$

The terminal power consists of the individual power contributions of the thyristor and MLCR rectifiers. The thyristor real power is thus:

$$P_{th} = \sqrt{3}k_{th}\left(\frac{3\sqrt{2}}{\pi}V_T\cos(\alpha_{th}) - \frac{3I_{d_{th}}X_c}{\pi}\right)I_{d_{th}} \tag{7.14}$$

which accounts for the average dc voltage reduction due to the commutation period and commutation reactance (X_c). With this topology, conversion constant k_{th} is approximately 1.4. The MLCR active power contribution is defined as:

$$P_R = \sqrt{3}k_RI_RV_T\cos(\alpha_R) \tag{7.15}$$

where MLCR constant k_R is the MLCR conversion ratio as given in equation 7.2. The reactive power demands of the thyristor rectifier is similarly calculated:

$$Q_{th} = \sqrt{3}k_{th}\left(\frac{3\sqrt{2}}{\pi}V_T\sin(\alpha_{th}) - \frac{3I_{d_{th}}X_c}{\pi}\right)I_{d_{th}} \tag{7.16}$$

The dc side equations given below are used to determine time constants for each of the current

controller parameter derivations. R_{dTH} and R_{dR} are comprised of the thyristor and MLCR rectifier's internal and switch on state losses respectively.

$$v_{dTH}(t) = R_{dTH} i_{dTH}(t) + L_{dTH} \frac{di_{dTH}(t)}{dt} + L_{dc} \frac{di_{dc}(t)}{dt} + V_o \tag{7.17}$$

$$v_{dR}(t) = R_{dR} i_{dR}(t) + L_{dR} \frac{di_{dR}(t)}{dt} + L_{dc} \frac{di_{dc}(t)}{dt} + V_o \tag{7.18}$$

Where V_o is the dc output voltage. Adding equations (7.17) and (7.18) together given that $I_{dTH} + I_{dR} = I_{dc}$ and $L_{dR} = L_{dTH}$, the relationships become:

$$\begin{aligned} v_{dR}(t) + v_{dTH}(t) = &\quad R_{dR} I_{dR}(t) + R_{dTH} I_{dTH}(t) + L_{dR} \left(\tfrac{di_{dR}(t)}{dt} + \tfrac{di_{dTH}(t)}{dt} \right) + 2L_{dc} \tfrac{di_{dc}(t)}{dt} + 2V_o \\ = &\quad R_{dR} I_{dR}(t) + R_{dTH} I_{dTH}(t) + (L_{dR} + 2L_{dc}) \tfrac{di_{dc}(t)}{dt} + 2V_o \end{aligned} \tag{7.19}$$

And rearranged to make $\frac{di_{dc}(t)}{dt}$ the subject:

$$\frac{di_{dc}(t)}{dt} = \frac{v_{dR}(t) + v_{dTH}(t) - R_{dR} I_{dR}(t) - R_{dTH} I_{dTH}(t) - 2V_o}{L_{dR} + 2L_{dc}} \tag{7.20}$$

which gives the relationship between the dc side parameters and the rate of current change.

The complete smelter model is thus shown in Figure 7.3.

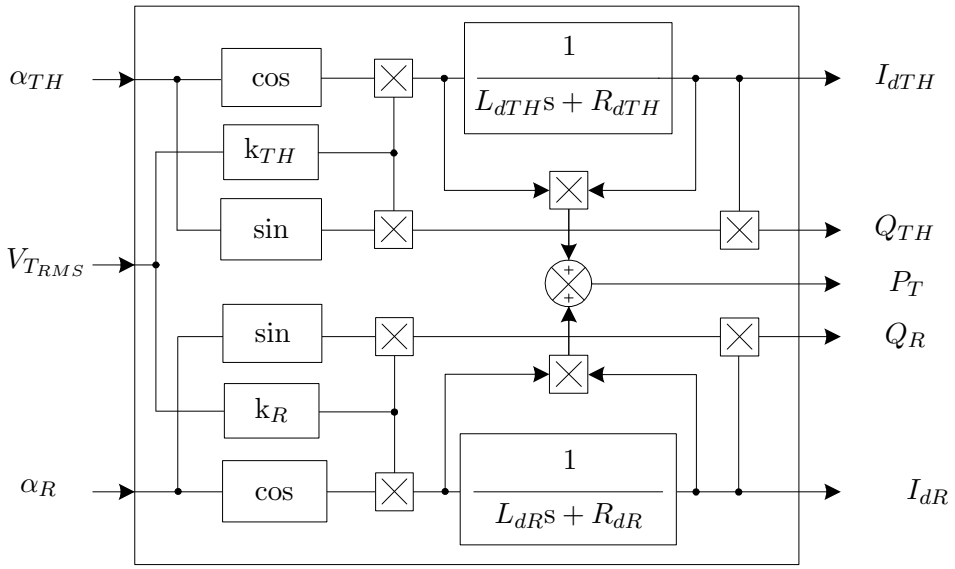


Figure 7.3 Smelter block diagram for control of real and reactive power

7.2.2 Control of the hybrid Thyristor-MLCR Smelter

A diagram of the controller for both the thyristor and MLCR rectifiers is given in Figure 7.4(a) and (b) respectively.

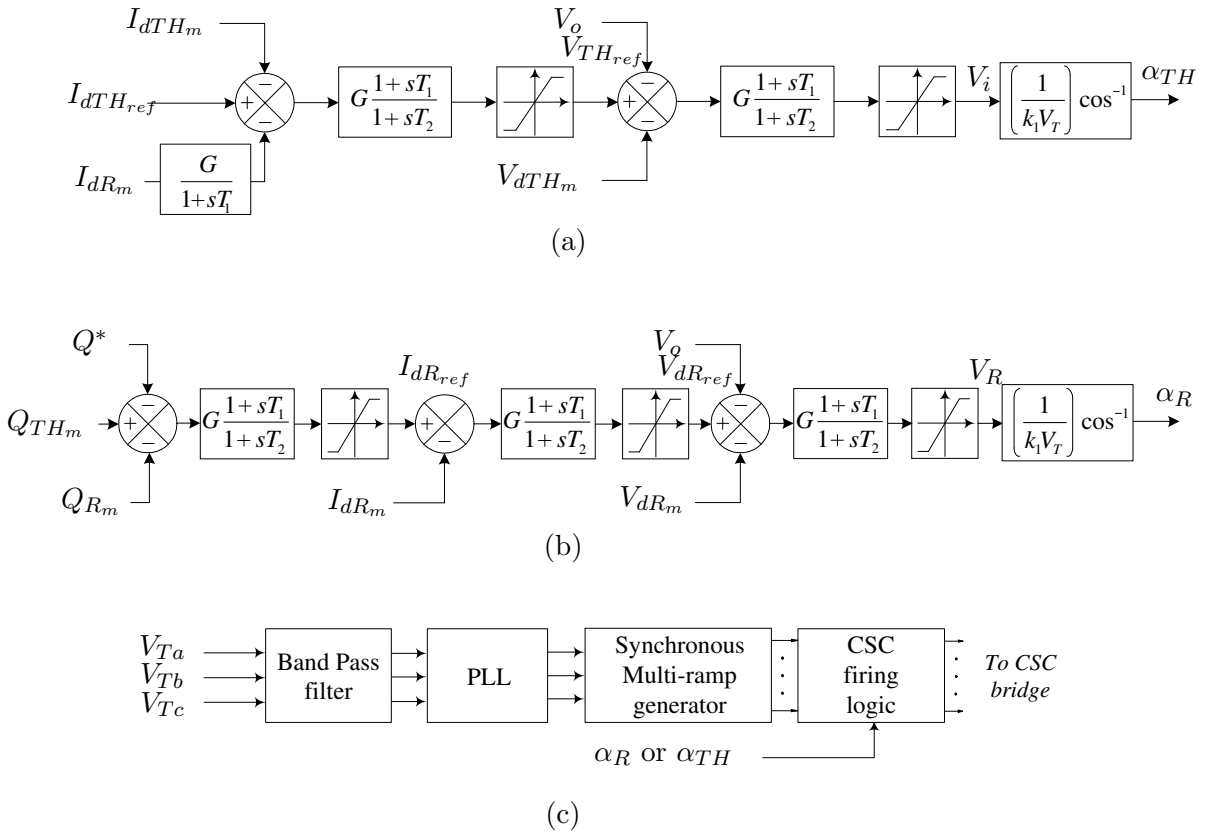


Figure 7.4 Controller layout for both the thyristor (a) and MLCR (b) bridges, with the common firing angle control in (c)

The thyristor rectifiers form the main current path in this configuration. Owing to the passive nature of the dc load, a single quadrant dc current control process provides sufficient controllability despite small fluctuations in load conditions. The dc current control loop in Figure 7.4(a) is common to all thyristor rectifiers, with a single firing angle command (α_{th}) used to preserve ideal phase-shift.

The dc current order ($I_{d_{thRef}}$) is compared to the measured thyristor dc current ($I_{d_{thm}}$), less the contribution of the reactive power compensation (given by $I_{d_{Rm}}$). The error signal is passed to a lead-lag compensator and the resulting signal is hard limited to prevent saturation, the output setting dc voltage control order $V_{d_{thref}}$. The closed loop bandwidth of the outer most dc current loop is a function of the dc side time constant, nominally 20-50Hz.

The thyristor inner control loop error signal is derived from the difference between dc voltage order ($V_{d_{thref}}$), measured dc voltage ($V_{d_{thm}}$) and dc back emf (represented by V_o), and is fed to

a second lead-lag compensator, the output of which is hard limited and scaled by the ac (RMS) terminal voltage (V_T). This incremental voltage is inverse cosined, resulting in firing angle order α_{th} which is sent to the thyristor firing logic, as given in Figure 7.4(c). Here, phase-locked loops (PLLs) are synchronised to each of the sinusoidal supply voltages ($V_{T_a} - V_{T_c}$) which generate the firing angle references for the six thyristors in each of the 12-pulse bridge rectifiers. The controller bandwidths for each of the 12-pulse dc voltage and firing angle loops are nominally $100 - 200$ Hz and 1 kHz respectively. Correction for the thyristor commutation angle isn't made directly in the dc voltage loop, as but the terminal voltage rms value is reduced with commutation, the inclusion of measured terminal voltage (V_T) in the inner control loop helps to minimise the non-linear effects.

The reactive power controller for the 48-pulse MLCR rectifier in Figure 7.4(b) has a similar configuration to that of the thyristor rectifier, with the addition of a third outer control loop for reactive power compensation. The error signal is derived from the difference between the measured reactive powers of the thyristor and MLCR rectifiers, with an optional boost order (Q^*) if additional reactive power generation is required. The error is then fed into a lead-lag compensator, its closed loop bandwidth approximately 10 Hz.

MLCR rectifier firing angle reference is developed using the same PLL as in 7.4(c), but the PLL is synchronised with the 3-phase ac terminal voltage taken from the LV side of the converter transformer. The MLCR supply current is quasi-sinusoidal and phase-shifts the LV terminal reference, and thus the true bridge supply voltage, depending on magnitude ac current, with MLCR operation so close to $|90°|$, establishing a true 90° reference relative to V_T is vital for stable operation.

As with the thyristor controller, the bandwidth of the MLCR PLL is 1kHz. The voltage control loop too, has the same control parameters its thyristor equivalent, but with its gain reduced proportional to the altered MLCR supply transformer ratio. The reinjection current control loop has the same format as its thyristor counterpart, but with a reduction in the dc inductance parameters due to the sinusoidal supply current and associated transformer phase-shift. This is shown in Figure 7.3 and equation 7.20.

The control of reactive power is inherently non-linear when related to firing angle (α_R), but as the firing angle is maintained near 90° (between $-90 \leq \alpha_R \leq -80°$ for a transformer ratio reduction of 10), over this small range the control behaviour is almost linear. The reactive power control works as follows; to increase reactive power generation (Q_R), I_{dR} needs to be increased. I_{dc} is maintained constant by reducing I_{dTH} which requires an increase in α_{TH} resulting in an increase in Q_{TH}. This process brings the smelter converter into a new operating state which is stable so long as controller interactions are damped. The main interaction path between the MLCR and thyristor controllers is via the measured MLCR dc current (I_{dR_m}) feed into the thyristor current controller. The effect is minimised by low pass filtering the feedback (I_{dR_m})

when used in the thyristor control. A large time constant is used, in most cases 100-200 mS is sufficient to decouple the responses.

7.3 DYNAMIC SIMULATION AND VERIFICATION

The simulated test system is shown in Figure 7.5. Four 12-pulse phase-shifted thyristor rectifiers make up the 48-pulse thyristor group, with each thyristor rectifier having its own zig-zag transformer, and phase-shifts of 0, 7.5, 15, 22.5° as indicated. The 48-pulse parallel MLCR rectifier is supplied via a 3-winding transformer with two secondaries configured in star and delta.

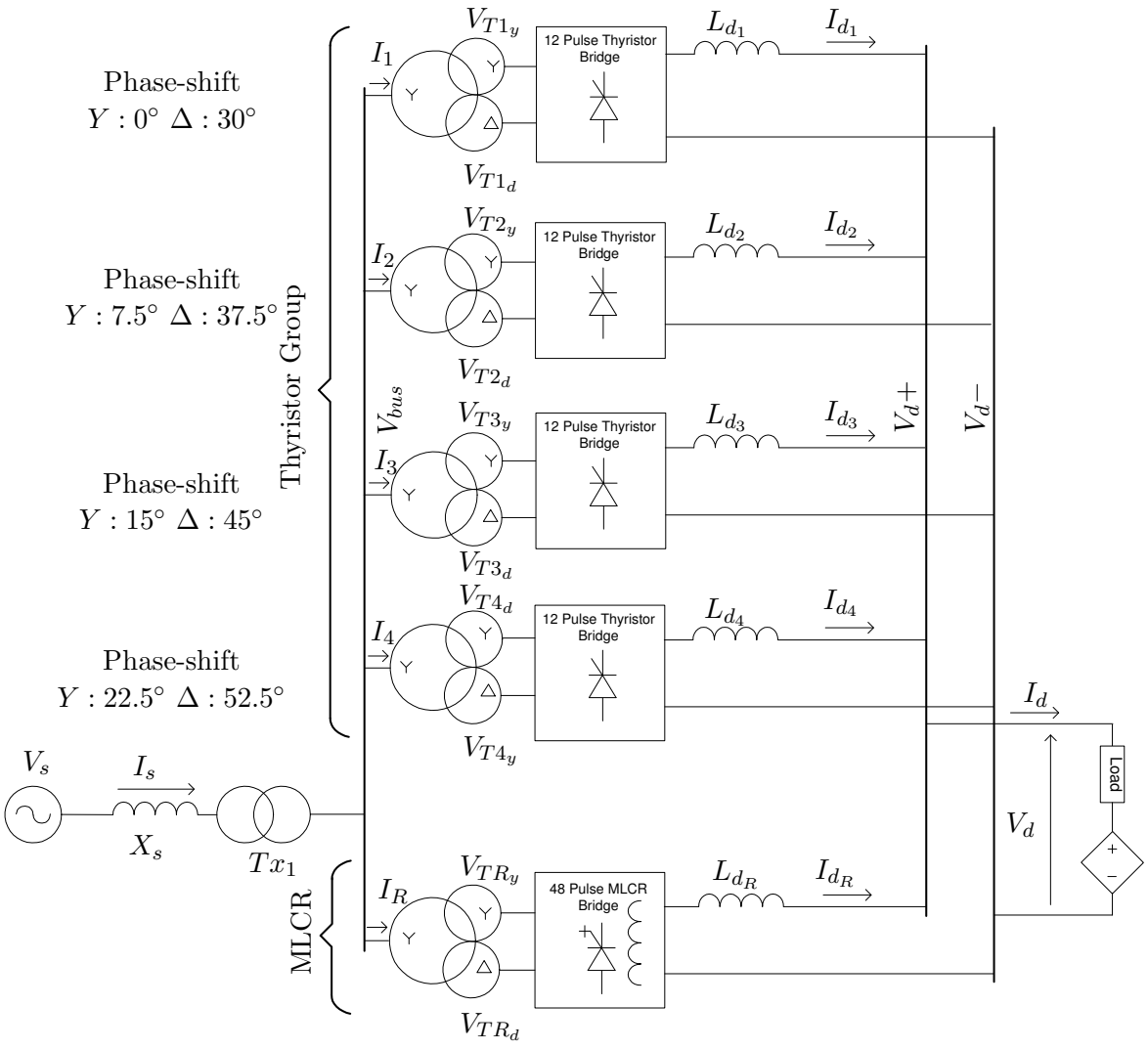


Figure 7.5 Paralleled test system comprised of four 12-pulse thyristor bridges and one 48-pulse MLCR bridge

The smelter circuit is simulated using the PSCAD/EMTDC package and its response to a series of step changes recorded. The step change magnitude and order of steps is designed to replicate a typical operating cycle in a smelting process, which may include commissioning, the cell warm

up process, normal production including cell removal for maintenance and smelter shut down.

The simulated time to full production has been compressed to make the dynamic simulation achievable. In practice the commissioning period is specified by how many cells are to be commissioned and how long each takes to reach operating temperature. A smelter consisting of 250 cells may take up to six months to commission when 1 to 2 cells are commissioned per day. In contrast, a restart may take half an hour if cell temperatures are near operating temperature.

It is assumed that during normal operation the smelter requires full dc current regardless of what proportion of the line is in service and that during commissioning the voltage is increased in stages until the whole smelter dc load is in service. Also, periodically some cells may be taken out of service for maintenance, with a maximum of $10 - 15\%$ removed.

7.3.1 Test system

The smelter is supplied at 220 kV by a thevenin source (V_s) through a system impedance (X_s), providing an SCR of 2.5. The main supply transformer (Tx_1) is rated at 200 MVA, 220:33 kV and feeds each of the thyristor phase-shifted transformers and the MLCR three-winding star-delta transformer, their secondary voltages being 0.8 kV and 7.6 kV respectively. The MLCR transformer ratio is calculated using equation (7.2), and all transformer leakage reactances are specified as 5%.

The dc load is rated at 1000 V and 160 kA with each 12-pulse thyristor bridge capable of delivering 40 kA at rated voltage. The smelter load is modelled as 250 series connected cells, with a total resistance of $4m\Omega$, inductance of 5.5 mH and back emf (V_o) of 320 V when all cells are in service.

7.3.2 Simulation Verification

The results of the simulation are given in Figure 7.6. The simulated smelter is initialised at 0.1s where the main thyristor groups are enabled with 20% of the installed dc load. The reactive power compensation is enabled at 1s and maintains unity power factor until its rating of 80 MVA is reached at 2s. The reactive power drawn from the system increases as dc current rises (in Figure 7.6(d)) until 95% of rated is reached at $t = 4.95s$ where a maximum of 46.5 MVAr and 40.5 MW (corresponding to a minimum power-factor of 0.65) is observed due to the large firing angle (graph (g)).

At $t = 5s$ additional cells are added to the smelter load in stages (15% at 0.5s intervals) until all cells are installed at 8.1s and full production commences. Note in graph 7.6(b) the reactive power demands steadily decrease from 5 to 8 seconds; then 85% of cells are installed and full

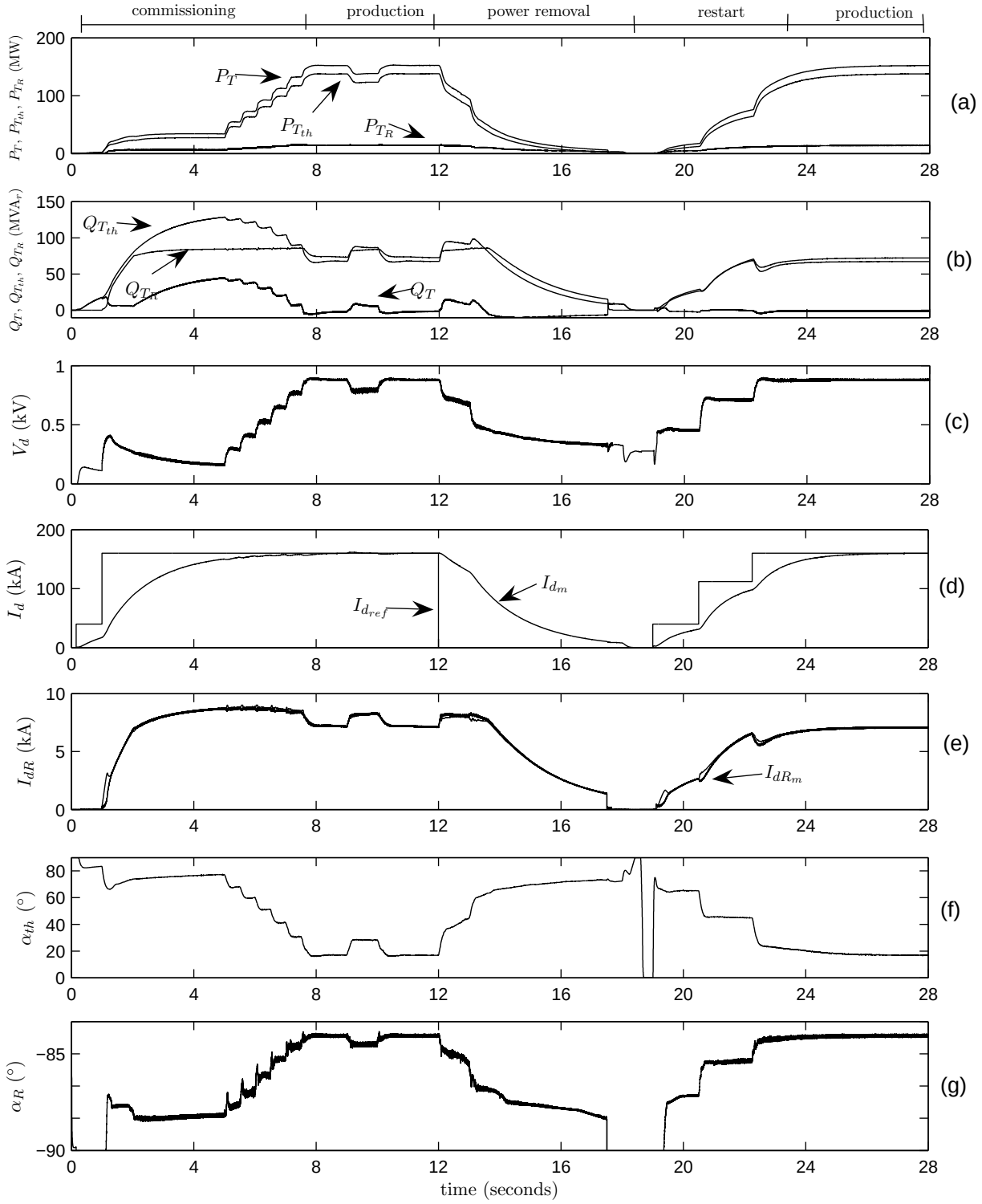


Figure 7.6 Operating response of a 160MW smelter converter over 28 second period

compensation is possible. The MLCR rectifier MVA output is sized for normal duty ($85-100\%$ installed cells at full load current) and thus during the commissioning period (1 s - 8 s) full compensation is not possible. The dc current contribution of the MLCR compensation, shown in graph 7.6(e), is 8.5 kA, with maximum real power of 14.5 MW, the firing angle to achieve this is maintained between -90° and $-83°$ as shown in Figure 7.6(f).

At $t = 9s$, 15% of the smelter load is short-circuited (to simulate the maximum number of cells removed for maintenance) and a corresponding reduction in dc voltage observed in graph (c). The dc current on the other hand remains constant in Figure 7.6(d). A small increase in Q_T is observed as the reactive power compensation once again is limited to its rated output; high power factor is maintained despite this, with a minimum terminal power-factor of 0.998 the result. At $t = 10s$ all cells are reinstated.

At $t = 12s$ the controlled removal of power begins. The dc current is reduced slowly, so that the absorption of excess reactive power is minimised. The reactive power absorbed by the thyristor bridges is initially larger than the rated MVA of the MLCR transformer and so power-factor drops momentarily to 0.985 lagging until compensation is made. DC current order is reduced further with the MLCR rectifier providing the necessary reactive power generation, a slight lag in the MLCR response producing a net reactive power surplus of -7 MVAr as seen from the converter terminal (graph (b) from 13.5 s to 17.5 s). Measured dc current falls to zero at 18.1 s, where both the thyristor and MLCR firing circuits are disabled, emulating a full smelter isolation from the ac power system.

The thyristor and MLCR rectifiers are re-enabled at t=19 s with the full compliment of smelter cells installed, a 20% dc current order is given, followed 2.5 s later by a 70% order, and finally 100% at 22.5 s. Full production resumes at 26 s.

7.3.3 Reactive power improvement during commissioning

During normal operation the hybrid converter has near unity power factor, and compensation takes place when a reduction in the number of cells occurs. High pulse and therefore ac current waveform quality is maintained across the entire operating range and the use of thyristors in the main dc current path ensures efficient performance.

The smelter commissioning phase however, may last for several months and a power factor of 0.65 is likely to be below the minimum permitted by the supply authority. Simply increasing the MLCR rectifier supply transformer rating and the ratio k_R would provide more compensation, but it may be more cost effective to install an additional 48-pulse MLCR rectifier with the same rating as the first. This would allow correction of twice the reactive power, which would be sufficient in this test case. Two MLCR rectifiers would only be required during commissioning,

but could also be used and provide common spare parts and full redundancy.

7.3.4 Harmonic performance

The harmonic performance of the smelter converter is taken during the normal operating portion of the simulation shown in Figure 7.6, between 8 and 9 seconds.

Phase-shifted Thyristor rectifier

The harmonic performance of the thyristor bridge is shown in Figure 7.7. One cycle of the current waveform is shown in (a) with the harmonic spectra for the first 200 order harmonics shown in (b). Very little distortion is present, with some low order harmonics of less than half a percent, and 48-pulse (47th, 49th) magnitude of 0.2%. Overall a THD of 1.04% results when the first 1000 harmonic orders are considered.

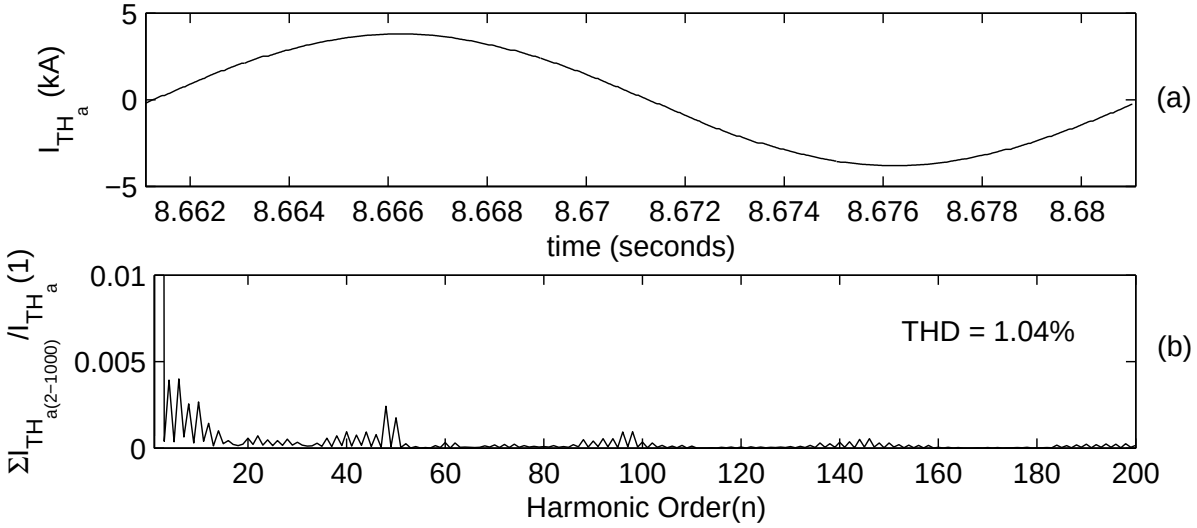


Figure 7.7 AC supply current waveform to the Thyristor branch and associated FFT

MLCR rectifier

In Figure 7.8, the MLCR bridge ac current has a maximum characteristic 48-pulse harmonic magnitude of 1.5%, with lesser magnitudes of 0.8% for the 12 and 96-pulse orders. Overall THD for the first 1000 harmonic orders is 2.9%. No effort has been made to optimise the snubbers on the reinjection circuit which may improve harmonic performance.

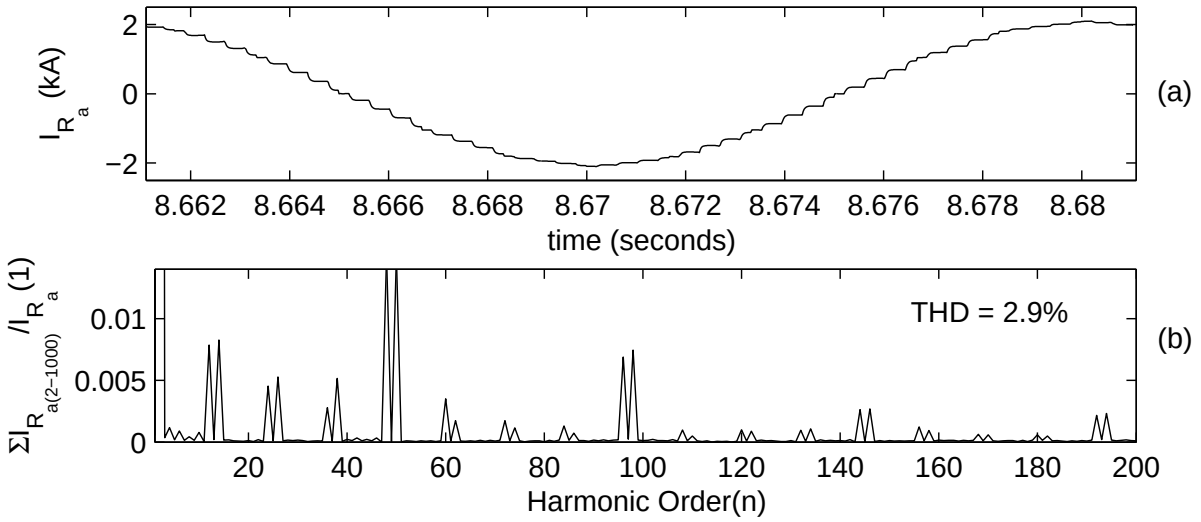


Figure 7.8 AC supply current waveform to the MLCR branch and associated FFT

Combined smelter harmonic performance

Overall the combination of the two converters with characteristic 48-pulse operation is given in Figure 7.9. Total harmonic distortion when considering the first 1000 harmonic orders is calculated at 1.82%. The waveform steps are less distinctive owing to the commutation overlap of the thyristor switches.

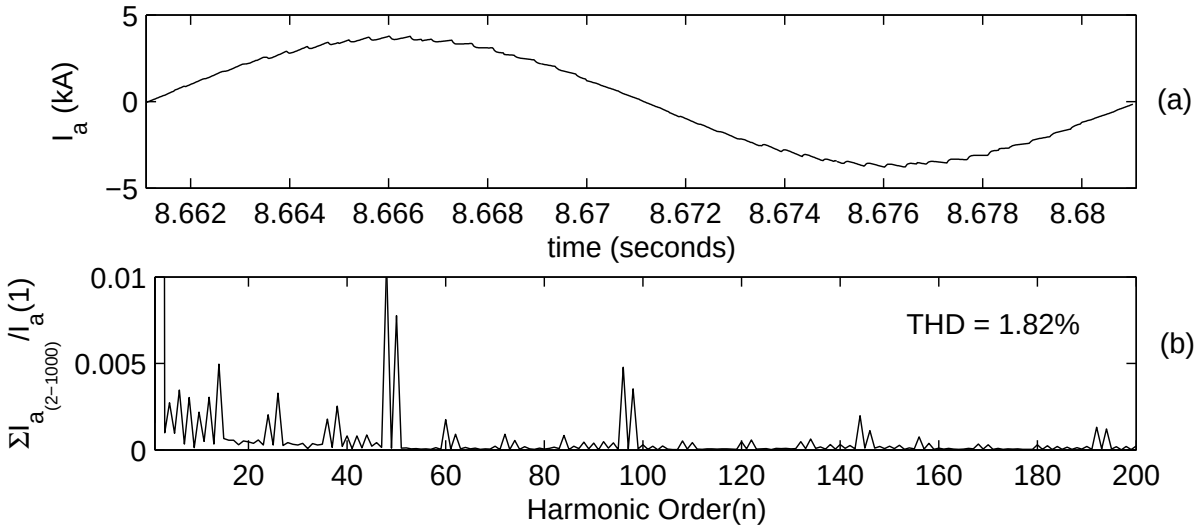


Figure 7.9 Combined AC supply current waveform to the Smelter and associated FFT

7.3.5 Hybrid Rectifier efficiency

Average efficiency of the thyristor rectifiers during normal operation is 96.1% from Figure 7.10(a), while the MLCR rectifier has a much lower average efficiency of 75% (in (b)), owing to the large transformer size (80 MVA) and relatively low active power output (14.5 MW). The efficiency is calculated conventionally, as the ratio of output power to input power.

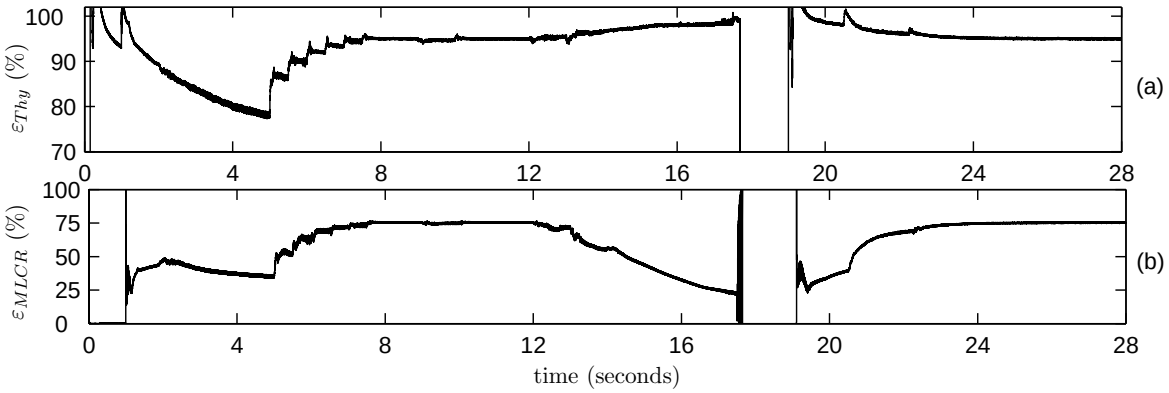


Figure 7.10 Efficiency comparison between the Thyristor and MLCR rectifiers

The combined efficiency is thus given as 93%, during normal operation, in Figure 7.11.

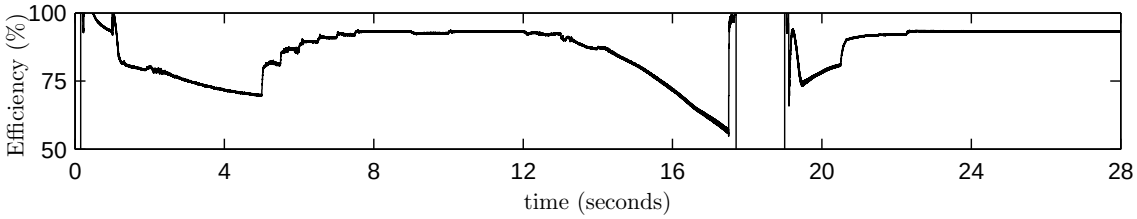


Figure 7.11 Combined efficiency of the Hybrid rectifier

Unlike the thyristor rectifier, the MLCR rectifier's prime purpose is to provide reactive power compensation, rather than active, and thus the conventional efficiency calculation is somewhat misleading. Published Statcom related papers [58, 59] state the real power losses in relation to total reactive power compensation capability. A summary of four of these configurations is given in Table 7.1.

The total losses of each topology are comprised of the Statcom switch on-state losses (GTOs), transformer resistive losses and simple snubber losses. Using this same method, the MLCR rectifier losses are summarised in Table 7.2. A total loss of 1.32% is marginally less than the True 48-pulse Statcom example, but much higher than either of the transformer-less examples (cascade and binary inverters). The three-winding transformer of the MLCR appears to contribute the main inefficiency, the copper losses scaling with transformer MVA rating.

Table 7.1 Losses of Four Statcom configurations

Converter Topology	True 48 pulse	Quasi-48-pulse	Cascade Inverter	Binary Inverter
Transformer losses	1.00%	1.42%	0.04%	0.04%
Converter losses	0.52%	0.59%	0.71%	0.79%
Total losses	1.52%	2.01%	0.75%	0.83%

Table 7.2 Calculated losses in the MLCR rectifier

MLCR rectifier	
Transformer losses	1.00%
Converter losses	0.32%
Total losses	1.32%

While Tables 7.1 and 7.2 provide an estimate of the real power losses, the switching frequency and strategy will contribute additional losses which neither table captures, as will the method of voltage balancing across the switches when many are series connected. This is particularly pertinent to the transformer-less topologies (Cascade Inverter and Binary Inverter in Table 7.1) as they are fed directly from the medium voltage bus and therefore require more series connected switches per phase.

The dynamic simulation of section 7.3.2 provides an accurate summation of all MLCR losses and is subsequently a much more realistic efficiency benchmark as switch dynamics are included, as are snubbers, non-linear transformer characteristics and control response. The MLCR losses may thus be compared for the reactive power rating of 80 MVAr using:

$$\text{Efficiency } (\%) = \left(1 - \frac{P_{T_R} - V_d I_{d_R}}{Q_{R_{rated}}}\right) \times 100\% \tag{7.21}$$

The revised efficiency is given in Figure 7.12.

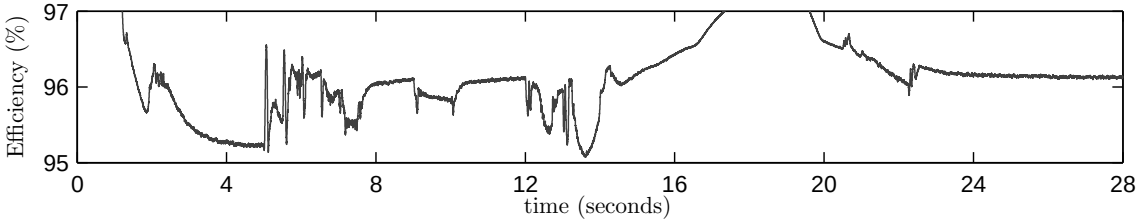


Figure 7.12 MLCR losses relative to Reactive power Rating

During normal operation this gives losses of 3.8% (almost three times that of Table 7.2), and an equivalent efficiency of 96.2%.

7.4 CONCLUSIONS

The MLCR rectifier provides full rated reactive power compensation that is virtually independent of smelter dc load conditions. The use of the multi-level reinjection current source rectifier ensures a high quality current waveform, and the coupling with the dc load reduces the losses associated with conventional dc side CSC Statcoms. The added complexity with a smelter dc interconnection will increase the installation costs and may make this configuration uneconomical in some situations. Similarly, the losses of the converter transformer make this topology less appealing as compared to accepted multi-level and multi-pulse voltage source alternatives.

Despite these apparent limitations, the use of thyristors and IGCTs, and the low-frequency switching required to achieve high pulse operation, may still make this a viable current sourced reactive power control alternative in very high-current applications.

Chapter 8

GENERAL CONCLUSIONS AND FUTURE WORK

8.1 GENERAL CONCLUSIONS

High efficiency is critical to the viability of very high power conversion. Conventional Line commutated (LCC) switching is the simplest and the most efficient, but suffers from low power-factor and affords no reactive power control flexibility.

For high efficiency, fundamental frequency switching is preferred, which prevents independent control of converter current amplitude and phase, as the converter firing angle affects both active and reactive powers. On-load tap-changing (OLTC) transformers are used in certain instances to step up or down ac terminal voltage to minimise firing angle, and thus reduce reactive power absorption, but these are costly and inefficient. Thus, although basic LCC efficiency is high, the auxiliary components required for reactive power compensation are complex and expensive, and lower overall converter efficiency.

At the voltage and current ratings considered for high power applications, multiple converters have to be series (high voltage) or parallel (high current) connected. Under conventional control this provides no increase in controllability, with traditionally all converters synchronised by a common firing angle. With the recent increases in ratings of self commutating (SCC) switches suitable for high power conversion, improved control strategies may be developed. As the firing angles of SCC are not constrained to a single operating quadrant, a converter may either generate or absorb reactive power. By connecting multiple current sourced converters (CSCs) to a common ac supply, individual converter firing angles may be shifted to control their summed ac current amplitude and phase, and thus achieve active and reactive power control independence.

This thesis has proposed a controllable firing-shift between series and parallel connected converters which is coordinated to give independent active and reactive power control. This concept gives thyristor convertors the control flexibility of PWM based topologies but with increased efficiency and rating. Control methods are developed for several HVDC transmission systems and very high dc current industrial processes, to match the four-quadrant and two-quadrant

load requirements respectively. The converter configurations have been extensively tested by EMTDC simulation, to characterise the dynamic behaviour, closed-loop control strategies and firing logic, and analyse the waveform quality.

The extra degree of freedom enabled under firing-shift control gives HVDC transmission the ability to separate active and reactive power control at each end of the dc link. Moreover, firing-shift control removes the reactive power interdependence between the sending and receiving ends, and eliminates the need for on-load tap-changers, two important limitations of conventional CSC links. In addition the increased controllability permits dc voltage to be fixed at rated level, thus minimising dc and ac current (and therefore losses) for all operating conditions. This added flexibility gives designers the freedom to directly control reactive power without reactive power compensation, for terminal voltage support, to improve network stability, or to increase transmission efficiency.

Using the Multi-level current reinjection (MLCR) converter as a base topology, the high-quality current waveform needs no harmonic filtering, and the multi-level reinjection ensures that the ac current is continuous, thus eliminating the costly ac capacitance interfacing to the grid. Without ancillary equipment for reactive and harmonic compensation, the converter station structure is simpler, and more flexible in terms of active and reactive power control than an LCC installation of the same rating.

The two-quadrant capability of very high current rectification is also proven with configurations based on phase-shifted 12-pulse and MLCR parallel CSCs. The elimination of the electro-mechanical OLTC/saturable reactor voltage control, the high-current CSC's biggest shortcoming, greatly improves controllability and with firing-shift control, ensures high power-factor for all load conditions. This reduces the reactive power demands on the transmission system, which results in more efficient power delivery.

The proposed high current applications, in both multi-pulse and multi-level configurations, produce high quality ac current waveforms under all load conditions, and suitable harmonic performance is achieved without harmonic filtering. The added dc current control flexibility of the parallel MLCR (and simplified transformer design), made possible by the high pulse output of each paralleled rectifier, gives additional reactive power control freedom, which may be used to further reduce ac system losses.

8.2 FUTURE WORK

The following topics need investigation to further exploit the firing shift concept in multi-level topologies.

8.2.1 Super conducting magnetic energy storage

The energy storage capability of super conducting magnetic energy storage (SMES) systems are being considered for large reactive power compensation and large active power load levelling applications, such as in large remote wind farms and photo-voltaic generation sites. A converter configuration with fast bidirectional power transfer is needed to connect the SMES to the ac system. With the super-cooled storage reactor considered a very large current source, and the need for full dc voltage and current control, a current sourced converter is the logical interface, in preference to an equivalent VSC which requires an additional dc chopper for dc voltage control.

The control flexibility of the 4-quadrant multi-level current reinjection CSCs proposed in this thesis provides an ideal foundation for an SMES interface to the grid. Under consideration are SMES schemes with over 1,000 kA dc, the voltage and current ratings obtained with suitable series and parallel MLCR configuration. The addition of a converter freewheeling operating state to the 4-quadrant controller (to maintain current flow when no power exchange is required) will enable effective exchange of active and reactive power between the SMES and the ac network.

8.2.2 Improved utilisation of parallel-MLCR reinjection switches

The parallel MLCR reinjection circuit switches have a high RMS rating but a lower average rating. The utilisation of the reinjection switches could be improved by an alternate reactor and switch configuration. By replacing the multi-tapped reactor with several parallel inductors, supplied by each bridge through its own self-commutated switch, each switches on-time may be extended and RMS current (and therefore rating) reduced. By having several switches conducting together, but staggering their switch-on instants the multi-level capability is retained.

8.2.3 MLCR laboratory prototype

The Multi-level current reinjection concept with thyristor main bridges has been simulated extensively using EMTDC/PSCAD package. With suitable switching of the reinjection circuit, the thyristors may be reverse biased for sufficient time to recover their blocking capability. The simplified switching model used in the simulation may not fully represent the switch characteristic and so conclusive proof of this concept requires the construction of a small-scale prototype.

The prototype could be built to test the validity of both the multi-level current and voltage reinjection schemes (MLCR and MLVR respectively) and further extended to verify the multi-group firing shift control concept of the MLCR.

Appendix A

PARALLEL CONNECTED MULTI-LEVEL CURRENT REINJECTION CONVERTER

The 48-pulse MLCR rectifier configuration used throughout this thesis is shown in Figure A.1. Two conventional 6-pulse bridge rectifiers ($S_{\Delta 1-6}$ and S_{Y1-6}) are parallel connected through an auxiliary circuit, which consists of reactors N_1 to N_4 and switches S_{j1} to S_{j5}.

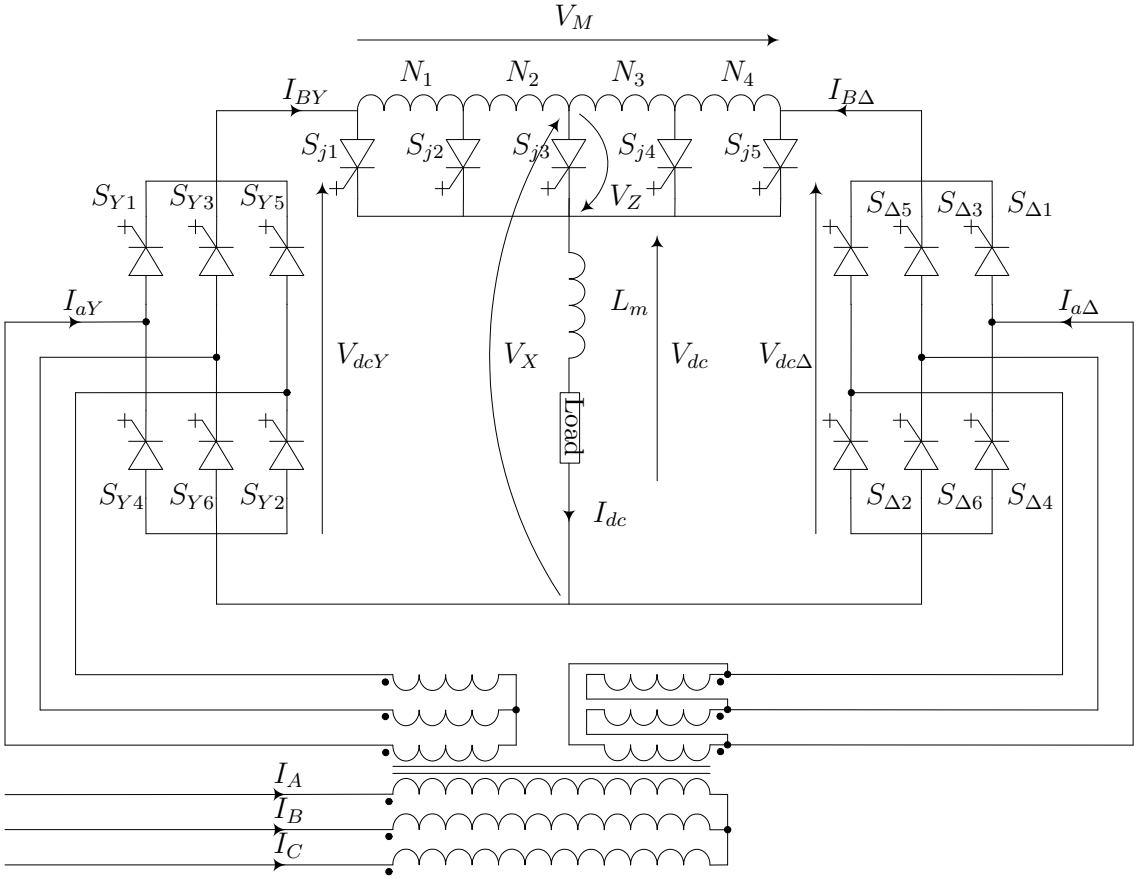


Figure A.1 5 level MLCR in Parallel configuration

This circuit switches at multiples of the supply frequency, properly distributing the dc load current between the main thyristor bridges, so that the current becomes a higher order, time

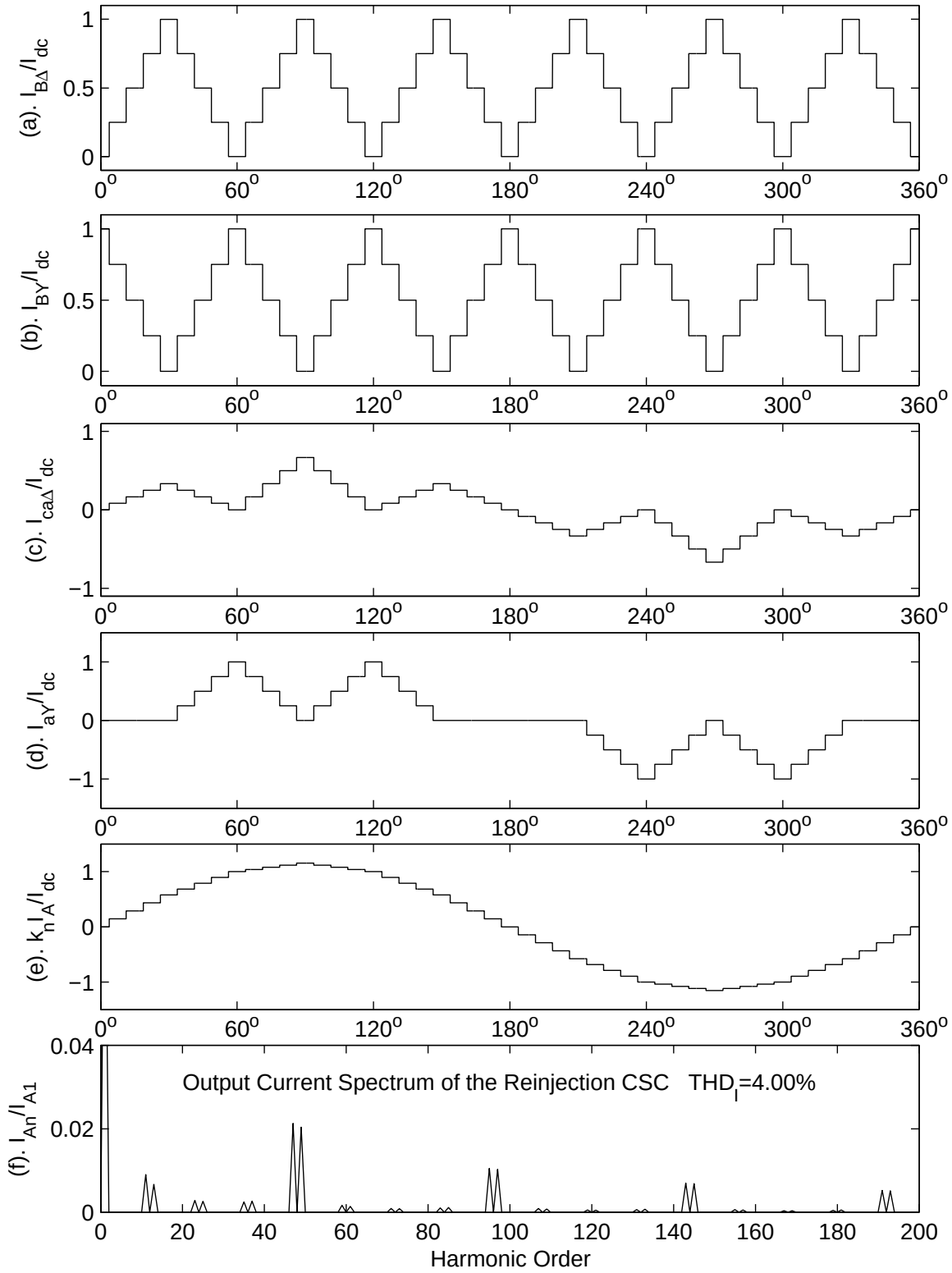


Figure A.2 Current Waveforms for a 5 level Parallel MLCR

varying function. The reinjection, rectifier bridges and total output current waveforms are shown in Figure A.2. As the reinjection switches operate at six times fundamental frequency the use of five levels should ideally produce a 60 pulse output (5(level number)×6(reinjection frequency)×2(number of bridges)). Moreover as explained in the literature, the reinjection switching can be controlled to force zero current regions during the main valve commutations. As shown in Figures A.2(a) to (e), a strategy that reduces the pulse number from 60 to 48.

Appendix B

SERIES CONNECTED MULTI-LEVEL CURRENT REINJECTION CONVERTER

The 5-level, 48-pulse series MLCR used in Chapters 2 and 4 of this thesis is given in Figure B.1.

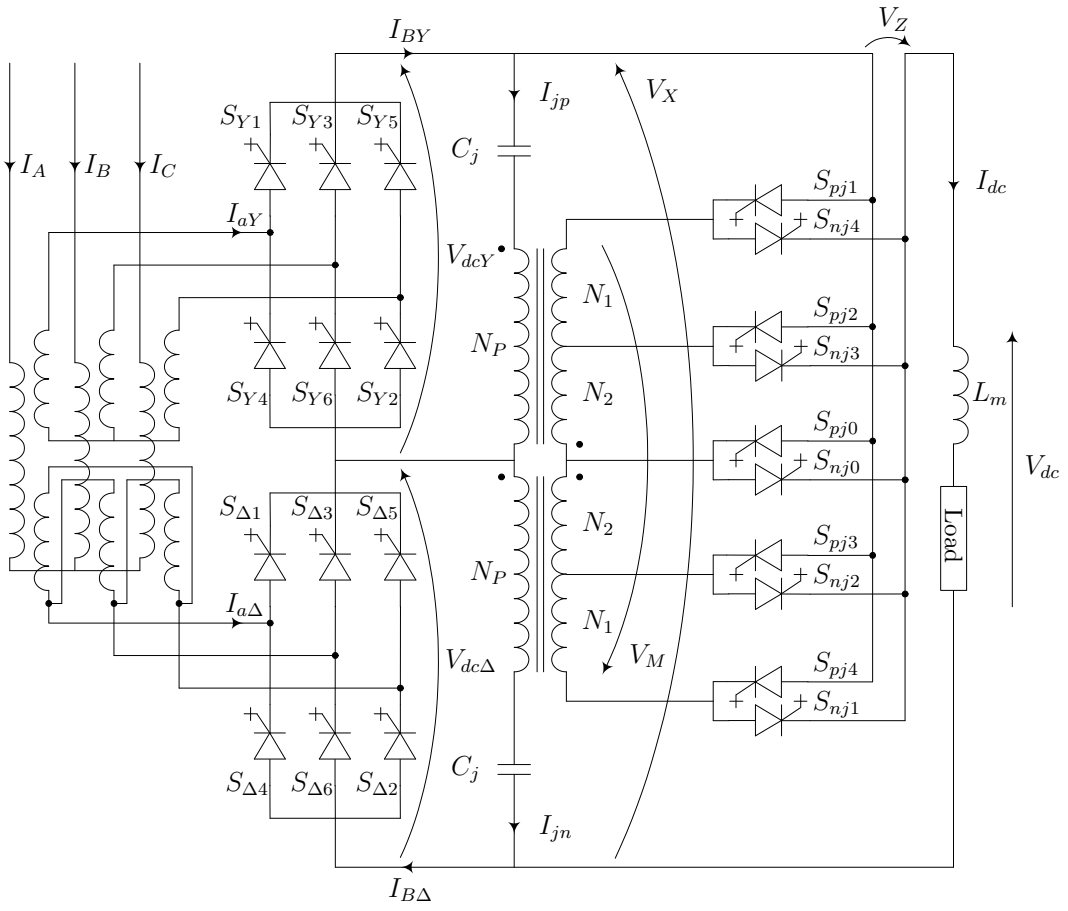


Figure B.1 5-level current reinjection CSC configuration

Two 6-pulse thyristor bridges are series connected, their ac supplies derived from separate star/delta and star/star windings as with standard 12-pulse thyristor based LCC converters. The reinjection scheme consists of switches $S_{pj1} - S_{pj4}$, $S_{nj1} - S_{nj4}$ and two identical single phase reinjection transformers with multi-tapped secondaries.

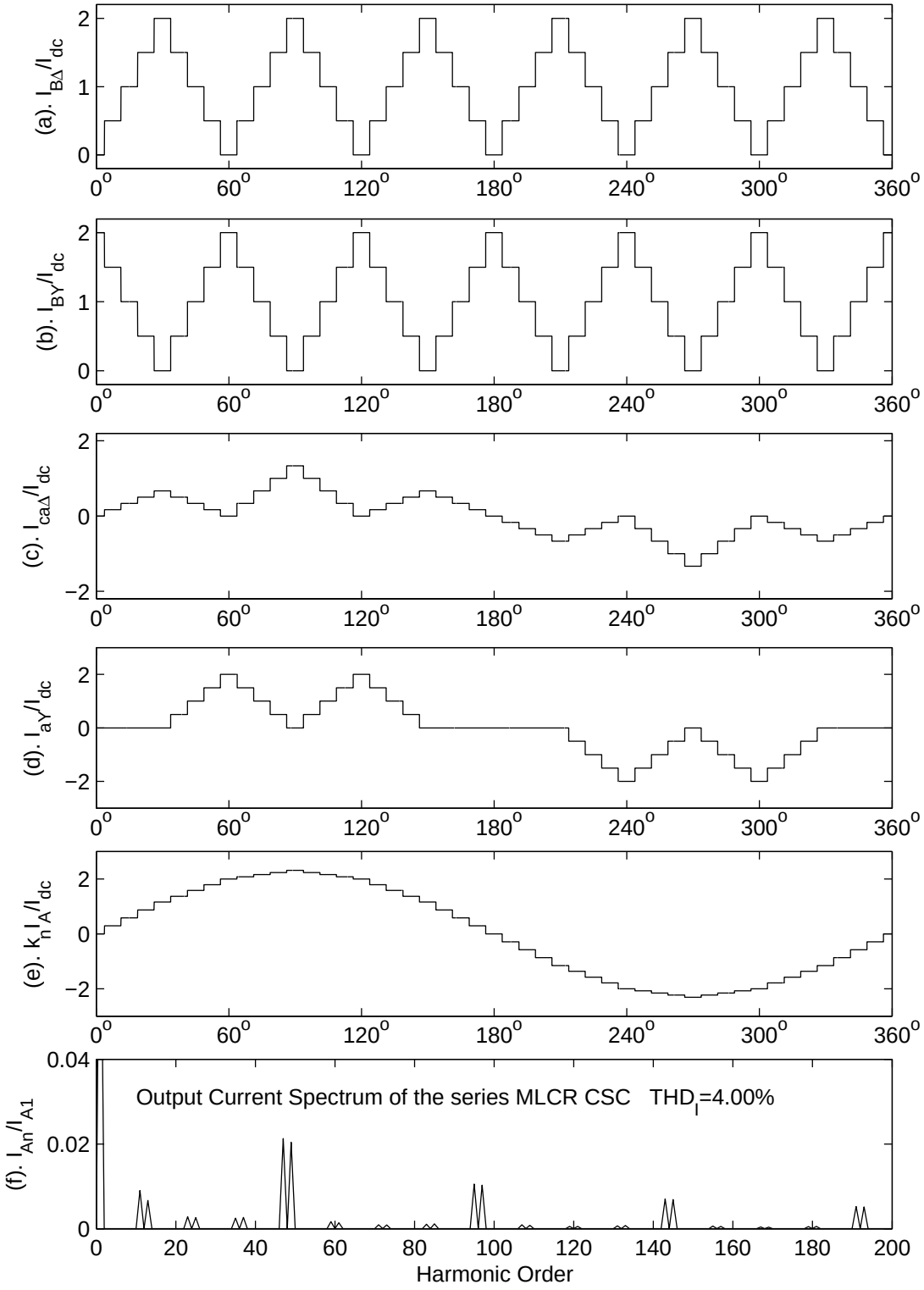


Figure B.2 Current waveforms of the MLCR-CSC

The dc load current circulates through the series connected reinjection switches, the secondary windings of the reinjection transformer and the inductive load. The dc current is sequentially switched at six times the fundamental frequency to produce stepped ac current waveforms (I_{jp}, I_{jn}) on the primary sides of the reinjection transformers. When the ac reinjection current is combined with the dc load current through dc blocking capacitors (C_j in Figure B.1), the resulting delta and star bridge waveforms may be seen in Figure B.2(a) and (b) respectively, with reference to one cycle of the ac supply current.

The ac current contributions of the star and delta connected bridge rectifiers are given in Figure B.2(c) and (d) respectively, and the resulting high-pulse ac supply current waveform over one cycle shown in B.2(e). The harmonic content of the supply current is given in Figure B.2(f), with a simulated THD of 3.16% over the first 200 harmonic orders.

Appendix C

PUBLICATIONS

The following is a list of publications resulting from the work described in this thesis.

1. N. J. Murray, J. Arrillaga, Y. H. Liu, and N. R. Watson, "Improved Simulation of an HVDC Test Case through Power-flow Initialisation," *International Conference on Power Systems Transients 2007*, IPST 07 - Lyon, France, June 4-7, 2007.

2. N. J. Murray, J. Arrillaga, Y. H. Liu, and N. R. Watson, "Flexible Reactive Power Control in Multigroup Current-Sourced HVDC Interconnections," *Power Delivery, IEEE Transactions on*, vol. 23, no. 4, pp. 21602167, 2008, 0885-8977.

3. N. J. Murray, J. Arrillaga, Y. H. Liu, and N. R. Watson, "Flexible Back-to-Back Power Conversion for Large Power System Interconnections," *accepted for publication in IET Power Electronics*

4. N. J. Murray, J. Arrillaga, Y. H. Liu, and N. R. Watson, "Two-Quadrant Power Control for Large-Current Low-Voltage Rectification with reference to Aluminium Smelters," *submitted for publication to IET Power Electronics.*

5. Y. H. Liu, J. Arrillaga, N. J. Murray, and N. R. Watson, "Derivation of a Four-Quadrant Control System For MLCR-HVDC Conversion," *submitted for publication to Power Delivery, IEEE Transactions on.*

REFERENCES

[1] W. Breuer, M. MLemes, and D. Retzmann, "Perspectives of HVDC and FACTS for system interconnection and Grid enhancement," *Brazil-China-India Summit Meeting on HVDC and Hybrid Systems: Planning and Engineering Issues*, p. 1 to 20, 2006.

[2] D. Retzmann and K. Uecker, "Benefits of HVDC and FACTS for sustainability and security of power supply," *Power Africa Conference and Exposition*, 2007.

[3] J. Rodriguez, L. Jih-Sheng, and P. Fang Zheng, "Multilevel inverters: a survey of topologies, controls, and applications," *Industrial Electronics, IEEE Transactions on*, vol. 49, no. 4, pp. 724–738, 2002, 0278-0046.

[4] T. Meynard and H. Foch, "Imbricated cell multi-level voltage source inverters for high voltage applications," *European Power Electronics Journal*, vol. 3(2), pp. 99–106, 1992.

[5] C. Hochgraf, R. Lasseter, D. Divan, and T. A. Lipo, "Comparison of multilevel inverters for static var compensation," *Conf. Rec. IEEE-IAS Annu. Meeting*, pp. pp. 921–928., 1994.

[6] A. Nabae, I. Takahashi, and H. Akagi, "A New Neutral-Point-Clamped PWM Inverter," *Industry Applications, IEEE Transactions on*, vol. IA-17, no. 5, pp. 518–523, 1981, 0093-9994.

[7] Y. Xiaoming and I. Barbi, "Fundamentals of a new diode clamping multilevel inverter," *Power Electronics, IEEE Transactions on*, vol. 15, no. 4, pp. 711–718, 2000, 0885-8993.

[8] K. Corzine and Y. Familiant, "A new cascaded multilevel H-bridge drive," *Power Electronics, IEEE Transactions on*, vol. 17, no. 1, pp. 125–131, 2002, 0885-8993.

[9] P. W. Hammond, "A new approach to enhance power quality for medium voltage drives," in *Petroleum and Chemical Industry Conference, 1995. Record of Conference Papers., Industry Applications Society 42nd Annual*, 1995, pp. 231–235.

[10] Y. H. Liu, J. Arrillaga, and N. R. Watson, "Cascaded H-Bridge Voltage Reinjection - Part I: A New Concept in Multilevel Voltage Source Conversion," *Power Delivery, IEEE Transactions on*, vol. 23, no. 2, pp. 1175–1182, 2008, 0885-8977.

[11] ——, "Cascaded H-Bridge Voltage Reinjection - Part II: Application to HVDC Transmission," *Power Delivery, IEEE Transactions on*, vol. 23, no. 2, pp. 1200–1206, 2008, 0885-8977.

[12] N. Stretch, M. Kazerani, and R. El Shatshat, "A Current-Sourced Converter-Based HVDC Light Transmission System," in *Industrial Electronics, 2006 IEEE International Symposium on*, vol. 3, 2006, pp. 2001–2006.

[13] K. Sadek, M. Pereira, D. P. Brandt, A. M. Gole, and A. Daneshpooy, "Capacitor commutated converter circuit configurations for DC transmission," *Power Delivery, IEEE Transactions on*, vol. 13, no. 4, pp. 1257–1264, 1998, 0885-8977.

[14] L. Carlsson, "Classical HVDC: still continuing to evolve," *Modern Power Systems*, 2002.

[15] J. Arrillaga, Y. H. Liu, and N. R. Watson, "Flexible Power Transmission - The HVDC Options," vol. John Wiley and Sons, West Sussex, England, 2007.

[16] J. F. Baird and J. Arrillaga, "Harmonic reduction in dc-ripple reinjection," *Proc. IEE*, vol. 127 pt. C, no. 5, pp. 294–303, 1980, 0018-9510.

[17] J. Arrillaga, Y. Liu, C. S. Crimp, and M. Villablanca, "Harmonic Reduction In Group-Connected Generators-HVDC Convertor," in *Harmonics in Power Systems., ICHPS V International Conference on*, 1992, pp. 202–207.

[18] Y. H. Liu, J. Arrillaga, and N. R. Watson, "Reinjection concept: A new option for large power and high-quality ac-dc conversion," *Power Electronics, IET*, vol. 1, no. 1, pp. 4–13, 2008, 1755-4535.

[19] E. P. Wiechmann, P. Aqueveque, A. S. Morales, P. F. Acuna, and R. Burgos, "Multicell High-Current Rectifier," *Industry Applications, IEEE Transactions on*, vol. 44, no. 1, pp. 238–246, 2008, 0093-9994.

[20] E. Wiechmann, R. Burgos, and J. Rodriguez, "High power factor phase controlled rectifier using staggered converters," in *Industry Applications Conference, 1997. Thirty-Second IAS Annual Meeting, IAS '97., Conference Record of the 1997 IEEE*, vol. 2, 1997, pp. 1390–1397 vol.2.

[21] J. R. Rodriguez, J. Pontt, C. Silva, E. P. Wiechmann, P. W. Hammond, F. W. Santucci, R. Alvarez, R. Musalem, S. Kouro, and P. Lezana, "Large current rectifiers: State of the art and future trends," *Industrial Electronics, IEEE Transactions on*, vol. 52, no. 3, pp. 738–746, 2005, 0278-0046.

[22] G. Asplund, K. Eriksson, and O. Tollerz, "Land and sea cable interconnections with hvdc light," *CEPSI 2000 conference, Manila, Philippines,*, vol. October 2000, 2000.

[23] G. Asplund, K. Eriksson, and K. Svensson, "DC transmission based on voltage source converters," *CIGRE SC Colloquium, Johannesburgh,S.A., 1977*, 1977.

[24] Cigre SC-4 WG 37, "VSC Transmission," *CIGRE SC-4, 2004*, 2004.

[25] N. S. Choi, J. G. Cho, and G. H. Cho, "A general circuit topology of multilevel inverter," in *Power Electronics Specialists Conference, 1991. PESC '91 Record., 22nd Annual IEEE*, 1991, pp. 96–103.

[26] L. B. Perera, N. R. Watson, Y. H. Liu, and J. Arrillaga, "Multilevel current reinjection self-commutated HVDC converter," *Generation, Transmission and Distribution, IEE Proceedings-*, vol. 152, no. 5, pp. 607–615, 2005, 1350-2360.

[27] J. Arrillaga, Y. H. Liu, L. B. Perera, and N. R. Watson, "A current reinjection scheme that adds self-commutation and pulse multiplication to the thyristor converter," *Power Delivery, IEEE Transactions on*, vol. 21, no. 3, pp. 1593–1599, 2006, 0885-8977.

[28] J. Graham, B. Jonsson, and R. Moni, "The Garabi 2000 MW Interconnection Back-to-Back HVDC to connect weak ac systems," *Trends on trans. sys. and telecoms, 2002 - library.abb.com*, 2002.

[29] A. M. H. A. Karim, N. H. A. Maskati, and S. Sud, "Status of Gulf co-operation council (GCC) electricity grid system interconnection," in *Power Engineering Society General Meeting, 2004. IEEE*, 2004, pp. 1385–1388 Vol.2.

[30] N. I. Voropai and Y. N. Kucherov, "Some aspects of Russian electricity policy taking into account the," in *Power Engineering Society Summer Meeting, 1999. IEEE*, vol. 2, 1999, pp. 615–618 vol.2.

[31] L. B. Perera, Y. H. Liu, N. R. Watson, and J. Arrillaga, "Multi-level current reinjection in double-bridge self-commutated current source conversion," *Power Delivery, IEEE Transactions on*, vol. 20, no. 2, pp. 984–991, 2005, 0885-8977.

[32] L. B. Perera, N. R. Watson, Y. H. Liu, and J. Arrillaga, "Multilevel current reinjection self-commutated HVDC converter," *Generation, Transmission and Distribution, IEE Proceedings-*, vol. 152, no. 5, pp. 607–615, 2005, 1350-2360.

[33] X. P. Zhang, C. Rehtanz, and Y. Song, "A grid for tomorrow," *Power Engineer (see also Power Engineering Journal)*, vol. 20, no. 5, pp. 22–27, 2006, 1479-8344.

[34] CIGRE WG 14.12, "System tests for HVDC installations." *E-CIGRE WG 14.12*, 1995.

[35] CIGRE WG 14.07, "Guide for planning DC links terminating at AC locations having low short-circuit capacities. Part 1. AC/DC interaction phenomena." *E-CIGRE WG 14.07*, 1992.

[36] P. Pollock and C. Duffey, "Power quality and corrective action in an aluminum smelter," in *Petroleum and Chemical Industry Conference, 1998. Industry Applications Society 45th Annual*, 1998, pp. 181–189.

[37] A. R. F. Williamson, J. Bekker, and D. A. Marshall, "Voltage quality improvements through capacitor bank tuning in the eskom transmission network," in *AFRICON, 1996., IEEE AFRICON 4th*, vol. 2, 1996, pp. 822–826 vol.2.

[38] C. T. Rim, N. S. Choi, G. C. Cho, and G. H. Cho, "A complete DC and AC analysis of three-phase controlled-current PWM rectifier using circuit D-Q transformation," *Power Electronics, IEEE Transactions on*, vol. 9, no. 4, pp. 390–396, 1994, 0885-8993.

[39] C. T. Rim, D. Y. Hu, and G. H. Cho, "Transformers as equivalent circuits for switches: general proofs and dq transformation-based analyses," *Industry Applications, IEEE Transactions on*, vol. 26, no. 4, pp. 777–785, 1990, 0093-9994.

[40] J. Salaet, S. Alepuz, A. Gilabert, and J. Bordonau, "Comparison between two methods of DQ transformation for single phase converters control. Application to a 3-level boost rectifier," in *Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual*, vol. 1, 2004, pp. 214–220 Vol.1.

[41] B. M. Han, G. G. Karady, J. K. Park, and S. I. Moon, "Interaction analysis model for transmission static compensator with emtp," *Power Delivery, IEEE Transactions on*, vol. 13, no. 4, pp. 1297–1302, 1998, 0885-8977.

[42] Y. B. Blauth and I. Barbi, "A phase-controlled 12-pulse rectifier with unity displacement factor without phase shifting transformer," in *Applied Power Electronics Conference and Exposition, 1998. APEC '98. Conference Proceedings 1998., Thirteenth Annual*, vol. 2, 1998, pp. 970–976 vol.2.

[43] T. Barton, "Rectifiers, Cycloconverters and AC Controllers," *Clarendon Press, Oxford*, 1994.

[44] M. P. Kazmierkowski and L. Malesani, "Current control techniques for three-phase voltage-source PWM converters: a survey," *Industrial Electronics, IEEE Transactions on*, vol. 45, no. 5, pp. 691–703, 1998, 0278-0046.

[45] J. Arrillaga and B. Smith, "AC-DC power system analysis," *Stevenage : Institution of Electrical Engineers, c1998.*, vol. IEE power and energy series ; 28, 1998.

[46] D. Paice, "Power electronic converter harmonics : multipulse methods for clean power," *Piscataway, NJ : IEEE Press, c1996.*, 1996.

[47] A. Molina, A. Gabaldon, F. Faura, and J. A. Fuentes, "New approaches to model electric demand in aluminium smelter industry," in *Industry Applications Conference, 2001. Thirty-Sixth IAS Annual Meeting. Conference Record of the 2001 IEEE*, vol. 2, 2001, pp. 1426–1431 vol.2.

[48] A. K. Malaviya and G. A. Bundell, "An intelligent controller for aluminum smelter potlines," *Industry Applications, IEEE Transactions on*, vol. 37, no. 3, pp. 792–805, 2001, 0093-9994.

[49] E. Wiechmann, R. Burgos, and J. Rodriguez, "High power factor phase controlled rectifier using staggered converters," in *Industry Applications Conference, 1997. Thirty-Second IAS Annual Meeting, IAS '97., Conference Record of the 1997 IEEE*, vol. 2, 1997, pp. 1390–1397 vol.2.

[50] ——, "Staggered phase controlled rectifier: a novel structure to achieve high power factor," in *Power Electronics Specialists Conference, 1997. PESC '97 Record., 28th Annual IEEE*, vol. 2, 1997, pp. 821–827 vol.2.

[51] E. P. Wiechmann, P. Aqueveque, A. S. Morales, P. F. Acuna, and R. Burgos, "Multicell high-current rectifier," *Industry Applications, IEEE Transactions on*, vol. 44, no. 1, pp. 238–246, 2008, 0093-9994.

[52] R. R. Brown, "Rectifier and dc bus system design for the copper electrowinning industry," *Industry Applications, IEEE Transactions on*, vol. 26, no. 6, pp. 1116–1119, 1990, 0093-9994.

[53] K. Bohnert, H. Brandle, M. G. Brunzel, P. Gabus, and P. Guggenbach, "Highly Accurate Fiber-Optic DC Current Sensor for the Electrowinning Industry," *Industry Applications, IEEE Transactions on*, vol. 43, no. 1, pp. 180–187, 2007, 0093-9994.

[54] L. B. Perera, Y. H. Liu, N. R. Watson, and J. Arrillaga, "Multi-level current reinjection in double-bridge self-commutated current source conversion," *Power Delivery, IEEE Transactions on*, vol. 20, no. 2, pp. 984–991, 2005, 0885-8977.

[55] Y. Qingguang, L. Pei, L. Wenhua, and X. Xiaorong, "Overview of STATCOM technologies," in *Electric Utility Deregulation, Restructuring and Power Technologies, 2004. (DRPT 2004). Proceedings of the 2004 IEEE International Conference on*, vol. 2, 2004, pp. 647–652 Vol.2.

[56] L. Jih-Sheng and P. Fang Zheng, "Multilevel converters-a new breed of power converters," *Industry Applications, IEEE Transactions on*, vol. 32, no. 3, pp. 509–517, 1996, 0093-9994.

[57] R. Grunbaum, "SVC Light: a powerful means for dynamic voltage and power quality control in industry and distribution," in *Power Electronics and Variable Speed Drives, 2000. Eighth International Conference on (IEE Conf. Publ. No. 475)*, 2000, pp. 404–409.

[58] T. Sato, Y. Matsushita, K. Temma, N. Morishima, and I. Iyoda, "Prototype test of STATCOM and BTB based on voltage source converter using GCT thyristor," in *Transmission and Distribution Conference and Exhibition 2002: Asia Pacific. IEEE/PES*, vol. 3, 2002, pp. 2037–2042 vol.3.

[59] C. K. Lee, J. S. K. Leung, S. Y. R. Hui, and H. S. H. Chung, "Circuit-level comparison of STATCOM technologies," *Power Electronics, IEEE Transactions on*, vol. 18, no. 4, pp. 1084–1092, 2003, 0885-8993.